中显液晶
技术资料

ANGLO JAPANESE AMERICAN AJA REGISTRARS ISO 9001 - 2000
UKAS QUALITY MANAGEMENT Reg. No. 059-A

中显控制器使用说明书

2009年3月15日

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RAiO

RA8835

Dot Matrix

LCD Controller

Specification

Version 1.2

May 18, 2005

RAiO Technology Inc.

Update History		
Version	**Date**	**Description**
1.0	March 23, 2005	Formal Release
1.1	April 28, 2005	Update Package Information: Figure 4-1, 4-2, Chapter 9-3, 9-4.
1.2	May 18, 2005	Update the index of Figure and Table

Chapter	Contents	Pages

1. Overview

The RA8835 is a controller IC that can display text and graphics on LCD panel. It can display layered text and graphics, scroll the display in any direction and partition the display into multiple screens. It also stores text, character codes and bitmapped graphics data in external frame buffer memory. Display controller functions include transferring data from the controlling microprocessor to the buffer memory, reading memory data, converting data to display pixels and generating timing signals for the buffer memory, LCD panel.

The RA8835 has an internal character generator with 160, 5x7 pixel characters in internal mask ROM. The character generators support up to 64, 8x16 pixel characters in external character generator RAM and up to 256, 8x16 pixel characters in external character generator ROM.

2. Features

- Text, graphics and combined text/graphics display modes
- Three overlapping screens in graphics mode
- Up to 640x256 pixel LCD panel display resolution
- Programmable cursor control
- Smooth horizontal and vertical scrolling of all or part of the display
- 1/2-duty to 1/256-duty LCD drive
- Up to 640x256 pixel LCD panel display resolution memory
- 160, 5x7 pixel characters in internal mask-programmed character generator ROM
- Up to 64, 8x16 pixel characters in external character generator RAM
- Up to 256, 8x16 pixel characters in external character generator ROM
- 6800 and 8080 family microprocessor interfaces
- Low power consumption—3.5 mA operating current (V_{DD} = 3.5V), 0.05μA standby current
- Package:
  RA8835P3N: QFP-60 pin (Lead Free)
  RA8835P4N: TQFP-60 pin (Lead Free)
- Power: 2.7 to 5.5 V

3. Block Diagram

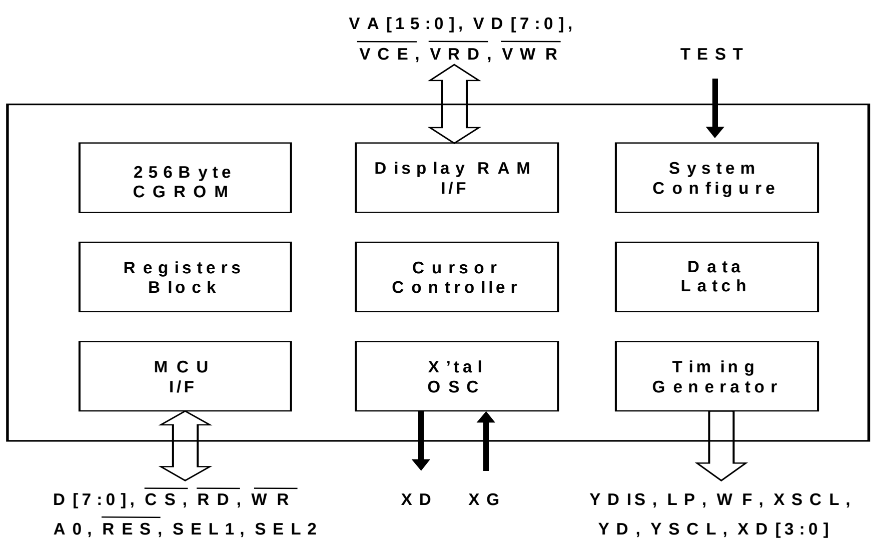


Figure 3-1: Block Diagram

4. Package

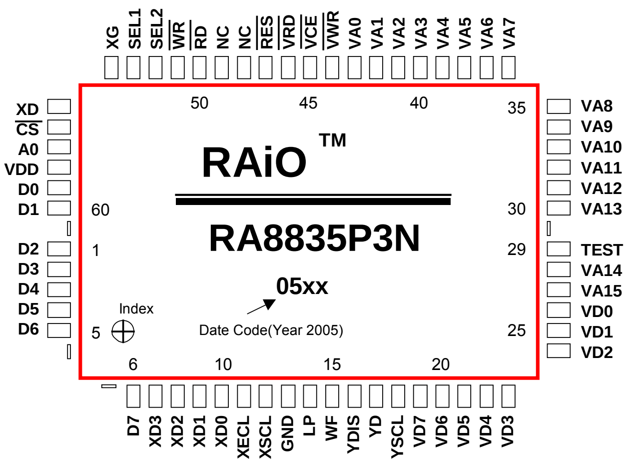


Figure 4-1: RA8835P3N(QFP-60 Pin)

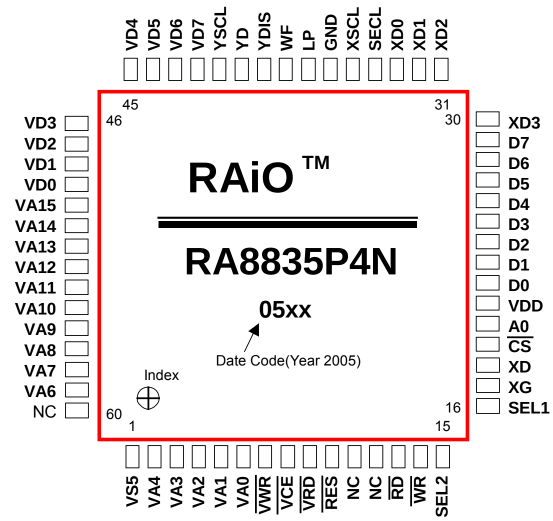


Figure 4-2: RA8835P4N (TQFP-60 Pin)

5. Pin Descriptions

5-1 Pin Functions

5-1-1 MCU Interface

<table>
<tr><th>Pin Name</th><th>Function</th></tr>
<tr><td>D0 to D7</td><td>MCU Data Bus.
Tristate input/output pins. Connect these pins to an 8- or 16-bit microprocessor bus.</td></tr>
<tr><td>SEL1, SEL2</td><td>MCU Interface Select.
The RA8835 series supports both 8080 family processors (such as the 8085 and Z80®) and 6800 family processors (such as the 6802 and 6809).
<table><tr><th>SEL1</th><th>SEL2*</th><th>Interface</th><th>A0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th></tr><tr><td>0</td><td>0</td><td>8080 family</td><td>A0</td><td>$\overline{RD}$</td><td>$\overline{WR}$</td><td>$\overline{CS}$</td></tr><tr><td>1</td><td>0</td><td>6800 family</td><td>A0</td><td>E</td><td>R/$\overline{W}$</td><td>$\overline{CS}$</td></tr></table>
SEL1 should be tied directly to VDD or VSS to prevent noise. If noise does appear on SEL1, decouple it to ground using a capacitor placed as close to the pin as possible.</td></tr>
<tr><td>$\overline{RD}$
or
E</td><td>Read Control or Enable.
When the 8080 family interface is selected, this signal acts as the active-LOW read strobe. The RA8835 series output buffers are enabled when this signal is active.
When the 6800 family interface is selected, this signal acts as the active-HIGH enable clock.
Data is read from or written to the RA8835 series when this clock goes HIGH.</td></tr>
</table>

<table>
<tr><td>$\overline{WR}$
or
$R/\overline{W}$</td><td>Write Control or Read/Write Control.
When the 8080 family interface is selected, this signal acts as the active-LOW write strobe. The bus data is latched on the rising edge of this signal.
When the 6800 family interface is selected, this signal acts as the read/write control signal. Data is read from the RA8835 series if this signal is HIGH, and written to the RA8835 series if it is LOW.</td></tr>
<tr><td>$\overline{CS}$</td><td>Chip Select.
This active-LOW input enables the RA8835 series. It is usually connected to the output of an address decoder device that maps the RA8835 series into the memory space of the controlling microprocessor.</td></tr>
<tr><td>A0</td><td>Command/Data Select.
8080 Family Interface:
<table>
<tr><th>A0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Status flag read</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Display data and cursor address read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Display data and parameter write</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Command write</td></tr>
</table>
6800 Family Interface:
<table>
<tr><th>A0</th><th>$R/\overline{W}$</th><th>E</th><th>Function</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Status flag read</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Display data and cursor address read</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Display data and parameter write</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Command write</td></tr>
</table></td></tr>
<tr><td>$\overline{RES}$</td><td>Hardware Reset.
This active-LOW input performs a hardware reset on the RA8835 series. It is an Schmitt-trigger input for enhanced noise immunity; however, care should be taken to ensure that it is not triggered if the supply voltage is lowered.</td></tr>
</table>

5-1-2 Display Memory Control

The RA8835 series can directly access static RAM and PROM. The designer may use a mixture of these two types of memory to achieve an optimum trade-off between low cost and low power consumption.

Pin Name	Function
VA0 to VA15	**16-bit Display Memory Address.** When accessing character generator RAM or ROM, VA0 to VA3, reflect the lower 4 bits of the RA8835 series' row counter.
VD0 to VD7	**Display Memory Data Bus.** 8-bit tristate display memory data bus. These pins are enabled when VR/(/W) is LOW.
$\overline{VWR}$	**Display Memory Write Control.** Active-LOW display memory write control output.
$\overline{VRD}$	**Display Memory Read Control.** Active-LOW display memory read control output.
$\overline{VCE}$	**Display Memory Chip Select.** Active-LOW static memory standby control signal. $\overline{VCE}$ can be used with $\overline{CS}$.

5-1-3 LCD Drive Signals

In order to provide effective low-power drive for LCD matrixes, the RA8835 series can directly control both the X- and Y-drivers using an enable chain.

Pin Name	Function
XD0 to XD3	**Data Output for Driver.** 4-bit X-driver (column drive) data outputs. Connect these outputs to the inputs of the X-driver chips.
XSCL	**Latch Clock.** The falling edge of XSCL latches the data on XD0 to XD3 into the input shift registers of the X-drivers. To conserve power, this clock halts between LP and the start of the following display line (See section 6-3-7).
XECL	**Trigger Clock for Chain Cascade.** The falling edge of XECL triggers the enable chain cascade for the X-drivers. Every 16th clock pulse is output to the next X-driver.
LP	**Latch Pulse.** LP latches the signal in the X-driver shift registers into the output data latches. LP is a falling-edge triggered signal, and pulses once every display line. Connect LP to the Y-driver shift clock on modules.
WF	**AC Drive Output.** The WF period is selected to be one of two values with SYSTEM SET command.
YSCL	**Latch Clock for YD.** The falling edge of YSCL latches the data on YD into the input shift registers of the Y-drivers. YSCL is not used with driver ICs that use LP as the Y-driver shift clock.
YD	**Data Pulse Output for Y Drivers.** It is active during the last line of each frame, and is shifted through the Y drivers one by one (by YSCL), to scan the display's common connections.
YDIS	**Power-down Output Signal.** YDIS is HIGH while the display drive outputs are active. YDIS goes LOW one or two frames after the sleep command is written to the RA8835 series. All Y-driver outputs are forced to an intermediate level (de-selecting the display segments) to blank the display. In order to implement power-down operation in the LCD unit, the LCD power drive supplies must also be disabled when the display is disabled by YDIS.

5-1-4 Oscillator and Power

Pin Name	Function
XG	**Crystal Connection for Internal Oscillator** This pin can be driven by an external clock source that satisfies the timing specifications of the EXT f0 signal (See section 7-3-6).
XD	**Crystal Connection for Internal Oscillator** Leave this pin open when using an external clock source.
VDD	**2.7 to 5.5V Supply.** This may be the same supply as the controlling microprocessor.
GND	**Ground**
TEST	**Test Pin.** This is a test pins. No need for connection(NC).

Note: The peak supply current drawn by the RA8835 series may be up to ten times the average supply current. The power supply impedance must be kept as low as possible by ensuring

that supply lines are sufficiently wide and by placing 0.47μF decoupling capacitors that have good high-frequency response near the device's supply pins.

5-2 RA8835 Pin Summary

Name	Number		Type	Description
	RA8835P3N	RA8835P4N		
VA0 to VA15	27 to 28 30 to 43	1 to 6 50 to 59	Output	VRAM address bus
$\overline{VWR}$	44	7	Output	VRAM write signal
$\overline{VCE}$	45	8	Output	Memory control signal
$\overline{VRD}$	46	9	Output	VRAM read signal
$\overline{RES}$	47	10	Input	Reset
NC	28, 48, 49	11, 12, 60	—	No connection
$\overline{RD}$	50	13	Input	8080 family: Read signal 6800 family: Enable clock (E)
$\overline{WR}$	51	14	Input	8080 family: Write signal 6800 family: $R/\overline{W}$ signal
SEL2	52	15	Input	8080 or 6800 family interface select
SEL1	53	16	Input	8080 or 6800 family interface select
XG	54	17	Input	Oscillator connection
XD	55	18	Output	Oscillator connection
$\overline{CS}$	56	19	Input	Chip select
A0	57	20	Input	Data type select
VDD	58	21	Supply	2.7 to 5.5V supply
D0 to D7	59 to 60 1 to 6	22 to 29	Input/output	Data bus
XD0 to XD3	7 to 10	30 to 33	Output	X-driver data
XECL	11	34	Output	X-driver enable chain clock
XSCL	12	35	Output	X-driver data shift clock
VSS	13	36	Supply	Ground
LP	14	37	Output	Latch pulse
WF	15	38	Output	Frame signal
YDIS	16	39	Output	Power-down signal when display is blanked
YD	17	40	Output	Scan start pulse
YSCL	18	41	Output	Y-driver shift clock
VD0 to VD7	19 to 26	42 to 49	Input/output	VRAM data bus

6. Instruction Set

6-1 The Command Set

Table-1: Command Set

Class	Command	Code											Hex	Command Description	Command Read Parameters	
		RD	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0			No. of Bytes	Section
System Control	**SYSTEM SET**	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8	9-2-1
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0	9-2-2
Display Control	**DISPLAY ON/OFF**	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable and disable display and display flashing	1	9-3-1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10	9-3-2
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2	9-3-3
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2	9-3-6
	CSRDIR	1	0	1	0	1	0	0	1	1	CD 1	CD 0	4C to 4F	Set direction of cursor movement	0	9-3-4
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	9-3-7
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	9-3-5
Drawing Control	**CSRW**	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	9-r1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2	9-4-2
Memory Control	**MWRITE**	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	—	9-5-1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	—	9-5-2

Notes:

1. In general, the internal registers of the RA8835 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged. 2-byte parameters (where two bytes are treated as 1 data item) are handled as follows:

   a. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.

   b. SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.

2. APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

6-2 System Control Commands

6-2-1 SYSTEM SET

Initializes the device, sets the window sizes, and selects the LCD interface format. Since this command sets the basic operating parameters of the RA8835 series, an incorrect SYSTEM SET command may cause other commands to operate incorrectly.

	MSB							LSB			
	D7	D6	D5	D4	D3	D2	D1	D0	A0	$\overline{WR}$	$\overline{RD}$
C	0	1	0	0	0	0	0	0	1	0	1
P1	0	0	IV	1	W/S	M2	M1	M0	0	0	1
P2	WF	0	0	0	0	← FX →			0	0	1
P3	0	0	0	0	← FY →				0	0	1
P4	← C/R →								0	0	1
P5	← TC/R →								0	0	1
P6	← L/F →								0	0	1
P7	← APL →								0	0	1
P8	← APH →								0	0	1

Figure 6-1: SYSTEM SET Instruction

6-2-1-1 C

This control byte performs the following:

1. Resets the internal timing generator
2. Disables the display
3. Cancels sleep mode

Parameters following P1 are not needed if only canceling sleep mode.

6-2-1-2 M0

Select the internal or external character generator ROM. The internal character generator ROM contains 160, 5 X 7 pixel characters, as shown in Figure 8-14. These characters are fixed at fabrication by the metallization mask.

The external character generator ROM, on the other hand, can contain up to 256 user-defined characters.
M0 = 0: Internal CG ROM
M0 = 1: External CG ROM

Note that if the CG ROM address space overlaps the display memory address space, that portion

of the display memory cannot be written to.

6-2-1-3 M1

Select the memory configuration for user-definable characters. The CG RAM codes select one of the 64 codes shown in figure 7-29.

M1 = 0: No D6 correction.
The CG RAM1 and CG RAM2 address spaces are not contiguous, the CG RAM1 address space is treated as character generator RAM, and the CG RAM2 address space is treated as character generator ROM.

M1 = 1: D6 correction.
The CG RAM1 and CG RAM2 address spaces are contiguous and are both treated as character generator RAM.

6-2-1-4 M2

Select the height of the character bitmaps. Characters more than 16 pixels high can be displayed by creating a bitmap for each portion of each character and using the RA8835 series graphics mode to reposition them.

M2 = 0: 8-pixel character height (2716 or equivalent ROM)
M2 = 1: 16-pixel character height (2732 or equivalent ROM)

6-2-1-5 W/S

Select the LCD drive method.

W/S = 0: Single-panel drive
W/S = 1: Dual-panel drive

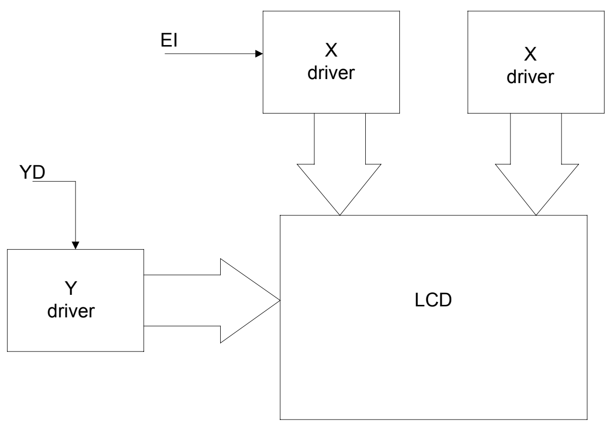


Figure 6-2: Single-panel Display

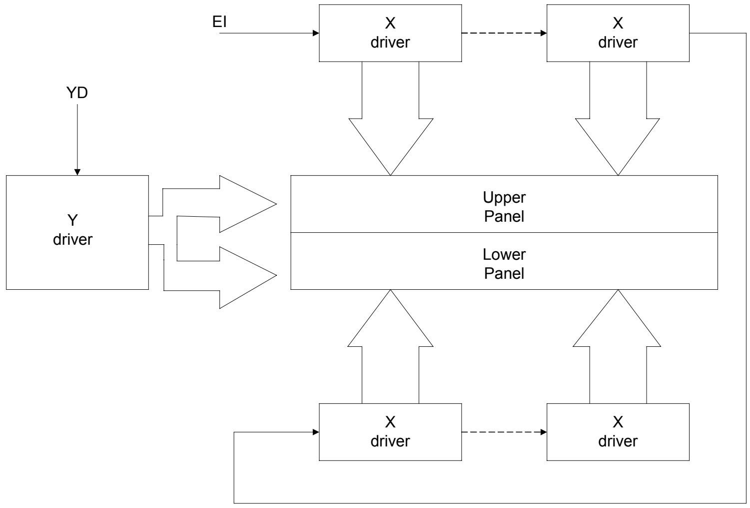


Figure 6-3: Above and Below Two-panel Display

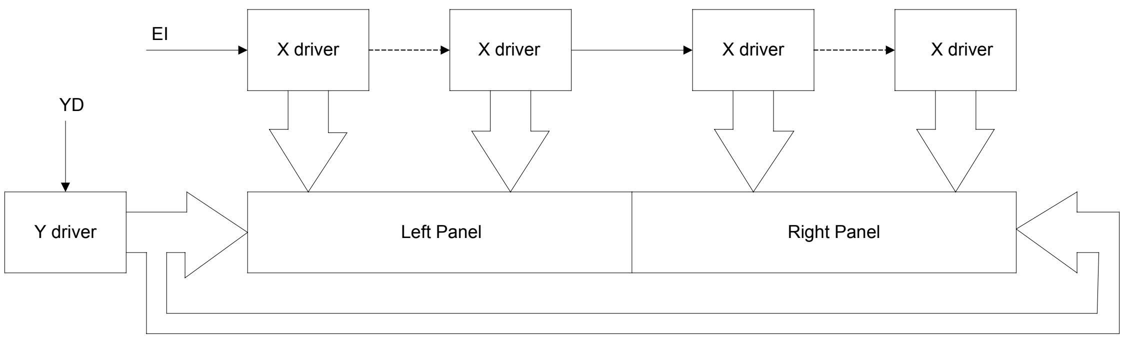


Figure 6-4: Left-and-Right Two-panel Display

Note:
There are no RAiO LCD units in the configuration shown in Figure 6-4.

Table-2: LCD Parameters

Parameter	W/S = 0		W/S = 1	
	IV = 1	IV = 0	IV = 1	IV = 0
C/R	C/R	C/R	C/R	C/R
TC/R	TC/R	TC/R (See note 1.)	TC/R	TC/R
L/F	L/F	L/F	L/F	L/F
SL1	00H to L/F	00H to L/F + 1 (See note 2.)	(L/F) / 2	(L/F) / 2
SL2	00H to L/F	00H to L/F + 1 (See note 2.)	(L/F) / 2	(L/F) / 2
SAD1	First screen block	First screen block	First screen block	First screen block
SAD2	Second screen block	Second screen block	Second screen block	Second screen block
SAD3	Third screen block	Third screen block	Third screen block	Third screen block
SAD4	Invalid	Invalid	Fourth screen block	Fourth screen block

Cursor movement range	Continuous movement over whole screen	Above-and-below configuration: continuous movement over whole screen

Notes:

1. See Table-24 for further details on setting the C/R and TC/R parameters when using
2. The value of SL when IV = 0 is equal to the value of SL when IV = 1, plus one.

6-2-1-6 IV

Screen origin compensation for inverse display. IV is usually set to 1. The best way of displaying inverted characters is to Exclusive-OR the text layer with the graphics background layer. However, inverted characters at the top or left of the screen are difficult to read as the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these characters.

The IV flag causes the RA8835 series to offset the text screen against the graphics back layer by one vertical pixel. Use the horizontal pixel scroll function (HDOT SCR) to shift the text screen 1 to 7 pixels to the right. All characters will then have the necessary surrounding background pixels that ensure easy reading of the inverted characters. See Section 11-5 for information on scrolling.

IV = 0: Screen top-line correction
IV = 1: No screen top-line correction

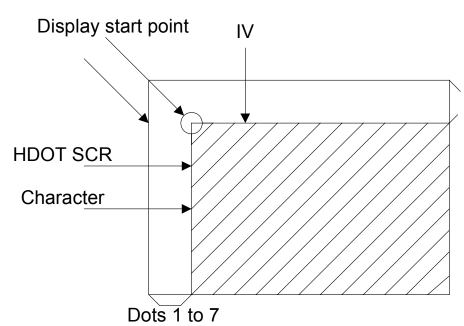


Figure 6-5: IV and HDOT SCR Adjustment

6-2-1-7 FX

Define the horizontal character size. The character width in pixels is equal to FX + 1, where FX can range from 00 to 07H inclusive. If data bit 3 is set (FX is in the range 08 to 0FH) and an 8-pixel font is used, a space is inserted between characters.

Table-3: Horizontal Character Size Selection

FX					[FX] character width (pixels)
HEX	**D3**	**D2**	**D1**	**D0**	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8

Since the RA8835 series handles display data in 8-bit units, characters larger than 8 pixels wide must be formed from 8-pixel segments. As Figure 6-6 shows, the remainder of the second eight bits are not displayed. This also applies to the second screen layer.

In graphics mode, the normal character field is also eight pixels. If a wider character field is used, any remainder in the second eight bits is not displayed.

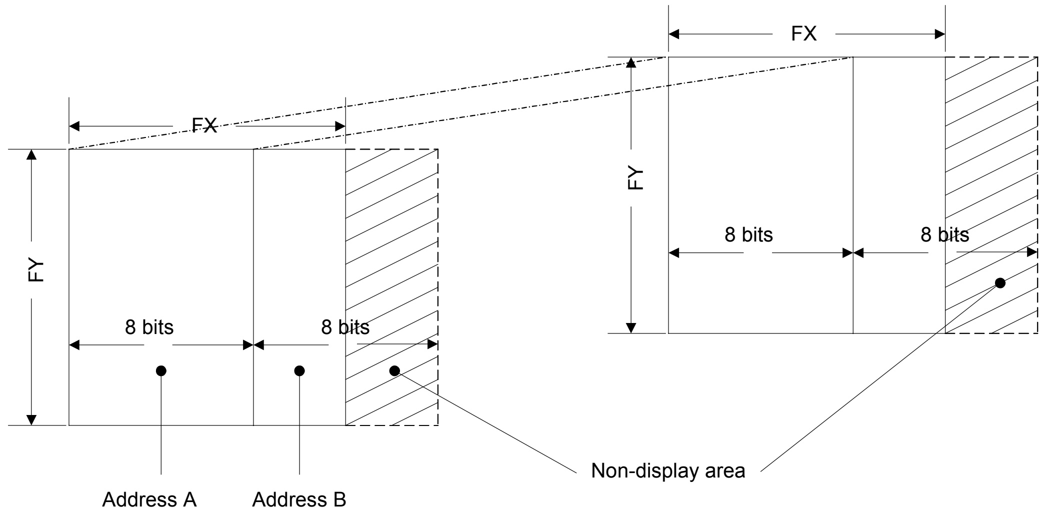


Figure 6-6: FX and FY Display Addresses

6-2-1-8 WF

Select the AC frame drive waveform period. WF is usually set to 1.
WF = 0: 16-line AC drive
WF = 1: two-frame AC drive
In two-frame AC drive, the WF period is twice the frame period.

In 16-line AC drive, WF inverts every 16 lines.
Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles.

6-2-1-9 FY

Set the vertical character size. The height in pixels is equal to FY + 1. FY can range from 00 to 0FH inclusive. Set FY to zero (vertical size equals one) when in graphics mode.

Table-4: Vertical Character Size Selection

FY					[FY] character height (pixels)
HEX	**D3**	**D2**	**D1**	**D0**	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8
↓	↓	↓	↓	↓	↓
0E	1	1	1	0	15
0F	1	1	1	1	16

6-2-1-10 C/R

Set the address range covered by one display line, that is, the number of characters less one, multiplied by the number of horizontal bytes per character. C/R can range from 0 to 239.

For example, if the character width is 10 pixels, then the address range is equal to twice the number of characters, less 2. See Section 17-1-1 for the calculation of C/R. [C/R] cannot be set to a value greater than the address range. It can, however, be set smaller than the address range, in which case the excess display area is blank. The number of excess pixels must not exceed 64.

Table-5: Display Line Address Range

C/R									[C/R] bytes per display line
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
4F	0	1	0	0	1	1	1	1	80
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
EE	1	1	1	0	1	1	1	0	239
EF	1	1	1	0	1	1	1	1	240

6-2-1-11 C/R

Set the length, including horizontal blanking, of one line. The line length is equal to TC/R + 1, where TC/ R can range from 0 to 255. TC/R must be greater than or equal to C/R + 4. Provided this condition is satisfied, [TC/R] can be set according to the equation given in section 17-1-1 in order to hold the frame period constant and minimize jitter for any given main oscillator frequency, f_{OSC}.

Table-6: Line Length Selection

TC/R									[TC/R] line length (bytes)
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
52	0	1	0	1	0	0	1	0	83
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

6-2-1-12 L/F

Set the height, in lines, of a frame. The height in lines is equal to L/F + 1, where L/F can range from 0 to 255.

Table-7: Frame Height Selection

L/F									[L/F] lines per frame
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

If W/S is set to 1, selecting two-screen display, the number of lines must be even and L/F must, therefore, be an odd number.

6-2-1-13 AP

Define the horizontal address range of the virtual screen. APL is the least significant byte of the address.

APL	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0
APH	AP15	AP14	AP13	AP12	AP11	AP10	AP9	AP8

Figure 6-7: AP Parameters

Table-8: Horizontal Address Range

Hex code				[AP] addresses per line
APH		APL		
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	0	5	0	80
↓	↓	↓	↓	↓
F	F	F	E	$2^{16} - 2$
F	F	F	F	$2^{16} - 1$

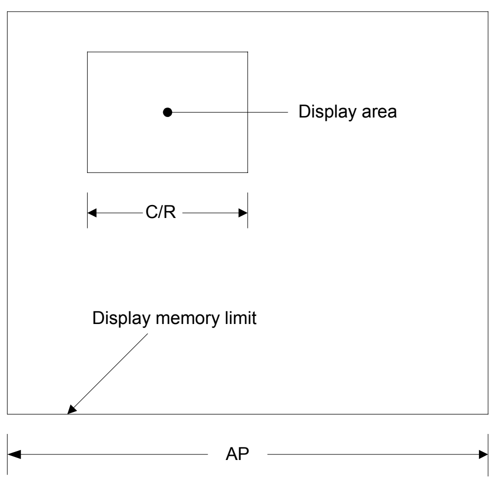


Figure 6-8: AP and C/R Relationship

6-2-2 SLEEP IN

Place the system in standby mode. This command has no parameter bytes. At least one blank frame after receiving this command, the RA8835 halts all internal operations, including the oscillator, and enters the sleep state.

Blank data is sent to the X-drivers, and the Y-drivers have their bias supplies turned off by the

YDIS signal. Using the YDIS signal to disable the Y-drivers guards against any spurious displays. The internal registers of the RA8835 series maintain their values during the sleep state. The display memory control pins maintain their logic levels to ensure that the display memory is not corrupted. The RA8835 series can be removed from the sleep state by sending the SYSTEM SET command with only the P1 parameter. The DISP ON command should be sent next to enable the display.

	MSB							LSB
C	0	1	0	1	0	0	1	1

Figure 6-9: SLEEP IN Instruction

1. The YDIS signal goes LOW between one and two frames after the SLEEP IN command is received. Since YDIS forces all display driver outputs to go to the deselected output voltage, YDIS can be used as a power-down signal for the LCD unit. This can be done by having YDIS turn off the relatively high power LCD drive supplies at the same time as it blanks the display.
2. Since all internal clocks in the RA8835 series are halted while in the sleep state, a DC voltage will be applied to the LCD panel if the LCD drive supplies remain on. If reliability is a prime consideration, turn off the LCD drive supplies before issuing the SLEEP IN command.
3. Note that, although the bus lines become high impedance in the sleep state, pull-up or pull-down resistors on the bus will force these lines to a known state.

6-3 Display Control Commands

6-3-1 DISP ON/OFF

Turn the whole display on or off. The single-byte parameter enables and disables the cursor and layered screens, and sets the cursor and screen flash rates. The cursor can be set to flash over one character or over a whole line.

	MSB							LSB
C	0	1	0	1	1	0	0	D
P1	FP5	FP4	FP3	FP2	FP1	FP0	FC1	FC0

Figure 6-10: DISP ON/OFF Parameters

6-3-1-1 D

Turn the display ON or OFF. The D bit takes precedence over the FP bits in the parameter.
D = 0: Display OFF
D = 1: Display ON

6-3-1-2 FC

Enables/disables the cursor and sets the flash rate. The cursor flashes with a 70% duty cycle (ON/OFF).

Table-9: Cursor Flash Rate Selection

FC1	FC0	Cursor display	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/64 Hz (approx. 1 Hz)

Note: As the MWRITE command always enables the cursor, the cursor position can be checked even when performing consecutive writes to display memory while the cursor is flashing.

6-3-1-3 FP

Each pair of bits in FP sets the attributes of one screen block, as follows. The display attributes are as follows:

Table-10: Screen Block Attribute Selection

FP1	FP0	First screen block (SAD1)	
FP3	FP2	Second screen block (SAD2, SAD4). See note.	
FP5	FP4	Third screen block (SAD3)	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

Note: If SAD4 is enabled by setting W/S to 1, FP3 and FP2 control both SAD2 and SAD4. The attributes of SAD2 and SAD4 cannot be set independently.

6-3-2 SCROLL

6-3-2-1 C

Set the scroll start address and the number of lines per scroll block. Parameters P1 to P10 can be omitted if not required. The parameters must be entered sequentially as shown in Figure 6-11.

	MSB							LSB	
C	0	1	0	0	0	1	0	0	
P1	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 1L)
P2	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 1H)
P3	L7	L6	L5	L4	L3	L2	L1	L0	(SL1)
P4	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 2L)
P5	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 2H)
P6	L7	L6	L5	L4	L3	L2	L1	L0	(SL2)
P7	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 3L)
P8	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 3H)
P9	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 4L)
P10	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 4H)

Figure 6-11: SCROLL Instruction Parameters

Note: Set parameters P9 and P10 only if both two-screen drive (W/S = 1) and two-layer configuration are selected. SAD4 is the fourth screen block display start address.

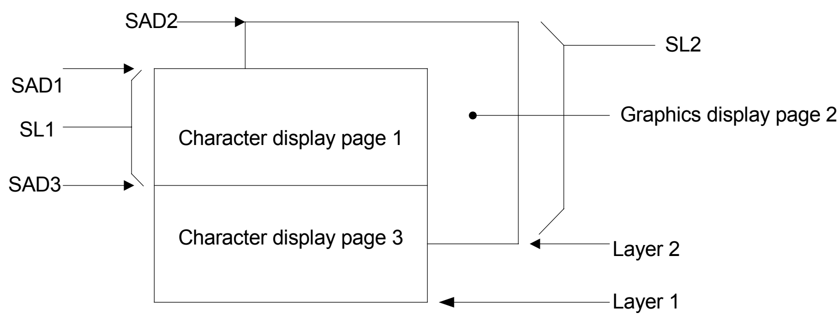
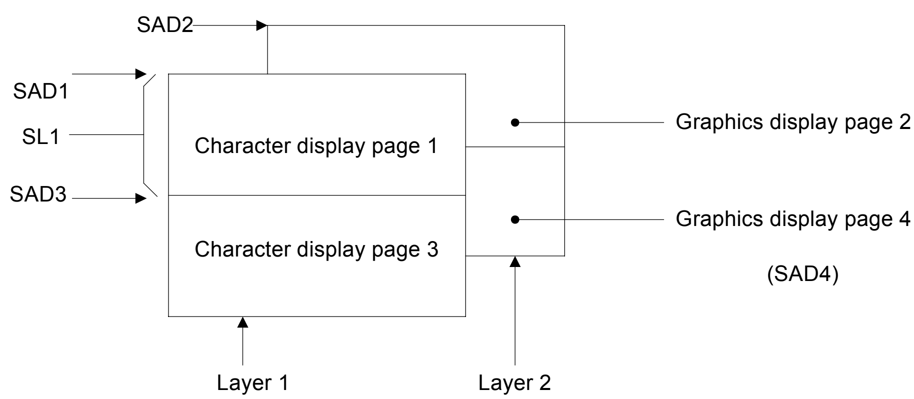
Table-11: Screen Block Start Address Selection

SL1, SL2									[SL] screen lines
HEX	**L7**	**L6**	**L5**	**L4**	**L3**	**L2**	**L1**	**L0**	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

6-3-2-2 SL1, SL2

SL1 and SL2 set the number of lines per scrolling screen. The number of lines is SL1 or SL2 plus one. The relationship between SAD, SL and the display mode is described below.

Table-12: Text Display Mode

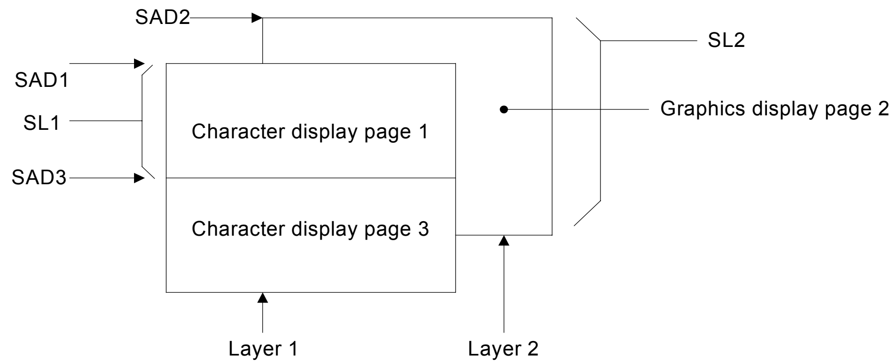
<table>
<tr><th>W/S</th><th>Screen</th><th>First Layer</th><th>Second Layer</th></tr>
<tr><td rowspan="4">0</td><td>First screen block</td><td>SAD1</td><td>SAD2</td></tr>
<tr><td>Second screen block</td><td>SL1</td><td>SL2</td></tr>
<tr><td>Third screen block (partitioned screen)</td><td colspan="2">SAD3 (see note 1)
Set both SL1 and SL2 to L/F + 1 if not using a partitioned screen.</td></tr>
<tr><td colspan="3">Screen configuration example:

</td></tr>
<tr><td rowspan="4">1</td><td>Upper screen</td><td>SAD1
SL1</td><td>SAD2
SL2</td></tr>
<tr><td>Lower screen</td><td>SAD3
(See note 2)</td><td>SAD4
(See note 2)</td></tr>
<tr><td colspan="3">Set both SL1 and SL2 to ((L/F) / 2 + 1)</td></tr>
<tr><td colspan="3">Screen configuration example:

</td></tr>
</table>

Notes:

1. SAD3 has the same value as either SAD1 or SAD2, whichever has the least number of lines (set by SL1 and SL2).
2. Since the parameters corresponding to SL3 and SL4 are fixed by L/F, they do not have to be set in this mode.

Table-13: Graphics Display Mode

W/S	Screen	First Layer	Second Layer	Third Layer
0	Two-layer composition	SAD1 SL1	SAD2 SL2	—
	Upper screen	SAD3 (see note 3) Set both SL1 and SL2 to L/F + 1 if not using a partitioned screen		—
	Screen configuration example:			



W/S	Screen	First Layer	Second Layer	Third Layer
0	Three-layer configuration	SAD1 SL1 = L/F + 1	SAD2 SL1 = L/F + 1	SAD3 —
	Screen configuration example:			

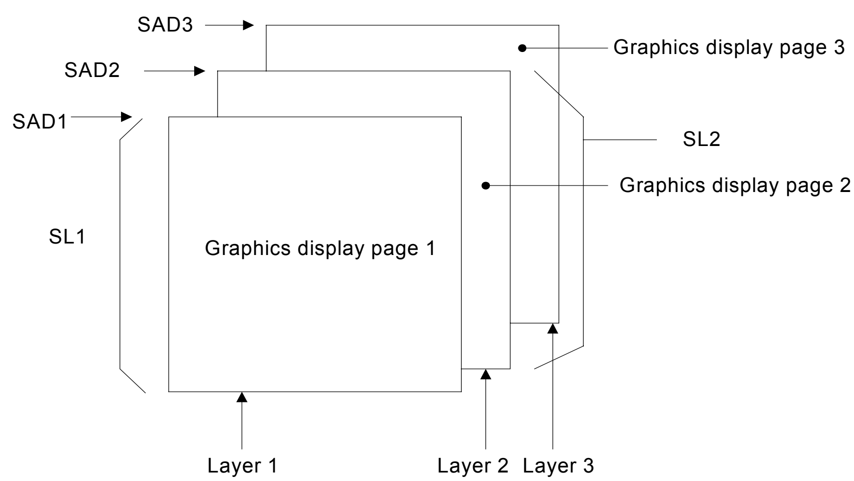
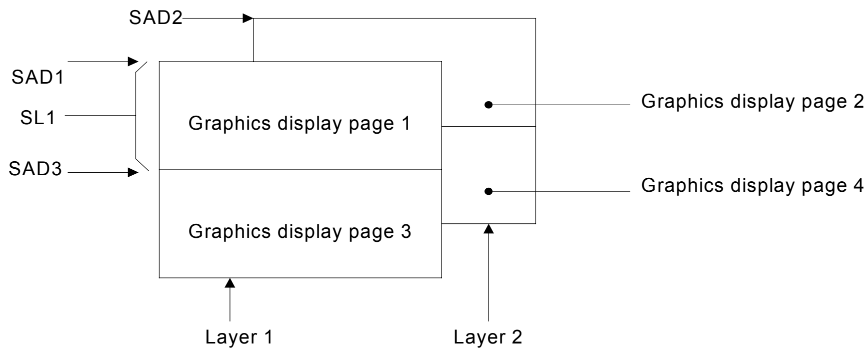


Table-13: Graphics Display Mode (continued)

W/S	Screen	First Layer	Second Layer	Third Layer
1	Upper screen	SAD1 SL1	SAD2 SL2	—
	Lower screen	SAD3 (See note 2)	SAD4 (See note 2)	—
	Screen configuration example (See note 3):			



Notes:

1. SAD3 has the same value as either SAD1 or SAD2; whichever has the least number of lines (set by SL1 and SL2).
2. Since the parameters corresponding to SL3 and SL4 are fixed by L/F, they do not have to be set.
3. If, and only if, W/S = 1, the differences between SL1 and (L/F + 1) / 2, and between SL2 and (L/F + 1) / 2, are blanked.

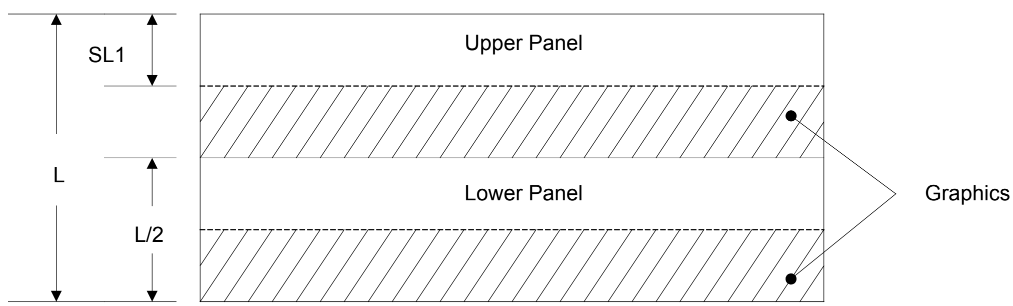


Figure 6-12: Two-panel Display Height

6-3-3 CSRFORM

Set the cursor size and shape. Although the cursor is normally only used in text displays, it may also be used in graphics displays when displaying special characters.

	MSB							LSB
C	0	1	0	1	1	1	0	1
P1	0	0	0	0	CRX X3	X2	X1	X0
P2	CM	0	0	0	CRY Y3	Y2	Y1	Y0

Figure 6-13: CSRFORM Parameter Bytes

6-3-3-1 CRX

Set the horizontal size of the cursor from the character origin. CRX is equal to the cursor size less one. CRX must be less than or equal to FX.

Table-14: Horizontal Cursor Size Selection

CRX					[CRX] cursor width (pixels)
HEX	**X3**	**X2**	**X1**	**X0**	
0	0	0	0	0	1
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
4	0	1	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

6-3-3-2 CRY

Set the location of an underscored cursor in lines, from the character origin. When using a block cursor, CRY sets the vertical size of the cursor from the character origin. CRY is equal to the number of lines less one.

Table-15: Cursor Height Selection

CRY					[CRY] cursor height (lines)
HEX	**Y3**	**Y2**	**Y1**	**Y0**	
0	0	0	0	0	Illegal
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
8	1	0	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

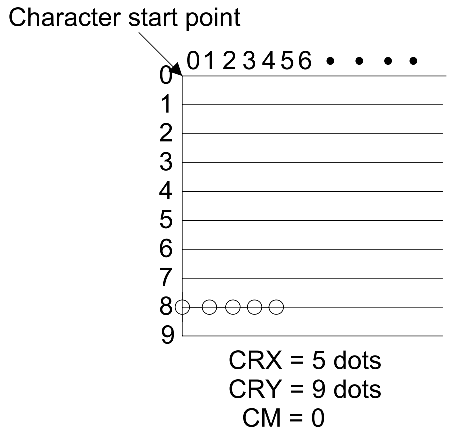


Figure 6-14: Cursor Size and Position

6-3-3-3 CM

Set the cursor shape. Always set CM to 1 when in graphics mode.
CM = 0: Underscore cursor
CM = 1: Block cursor

6-3-4 CSRDIR

Set the direction of automatic cursor increment. The cursor can move left or right one character, or up or down by the number of bytes specified by the address pitch, AP. When reading from and writing to display memory, this automatic cursor increment controls the display memory address increment on each read or write.

	MSB							LSB
C	0	1	0	0	1	1	CD1	CD2

Figure 6-15: CSRDIR Parameters

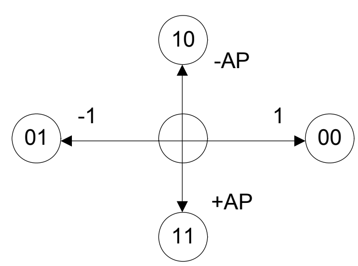


Figure 6-16: Cursor Direction

Table-16: Cursor Shift Direction

C	CD1	CD0	Shift direction
4CH	0	0	Right
4DH	0	1	Left

4EH	1	0	Up
4FH	1	1	Down

Note: Since the cursor moves in address units even if $FX \geq 9$, the cursor address increment must be preset for movement in character units. See Section 10-3.

6-3-5 OVLAY

Selects layered screen composition and screen text/ graphics mode.

	MSB							LSB
C	0	1	0	1	1	0	1	1
P1	0	0	0	OV	DM2	DM1	MX1	MX0

Figure 6-17: OVLAY Parameters

6-3-5-1 MX0, MX1

MX0 and MX1 set the layered screen composition method, which can be either OR, AND, Exclusive-OR or Priority- OR. Since the screen composition is organized in layers and not by screen blocks, when using a layer divided into two screen blocks, different composition methods cannot be specified for the individual screen blocks. The Priority-OR mode is the same as the OR mode unless flashing of individual screens is used.

Table-17: Composition Method Selection

MX1	MX0	Function	Composition Method	Applications
0	0	$L1 \cup L2 \cup L3$	OR	Underlining, rules, mixed text and graphics
0	1	$(L1 \oplus L2) \cup L3$	Exclusive-OR	Inverted characters, flashing regions, underlining
1	0	$(L1 \cap L2) \cup L3$	AND	Simple animation, three-dimensional appearance
1	1	L1 > L2 > L3	Priority-OR	

Notes:

L1: First layer (text or graphics). If text is selected, layer L3 cannot be used.
L2: Second layer (graphics only)
L3: Third layer (graphics only)

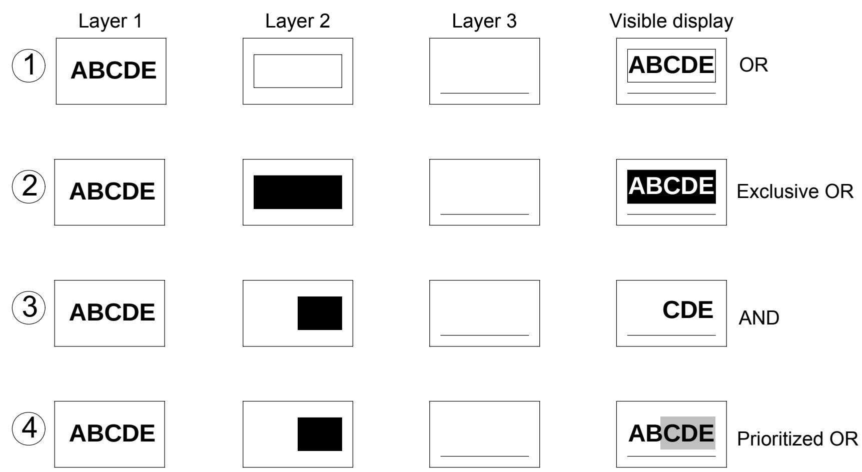


Figure 6-18: Combined Layer Display

Notes:

L1: Not flashing
L2: Flashing at 1 Hz
L3: Flashing at 2 Hz

6-3-5-2 DM1, DM2

DM1 and DM2 specify the display mode of screen blocks 1 and 3, respectively.
DM1/2 = 0: Text mode
DM1/2 = 1: Graphics mode

Note 1: Screen blocks 2 and 4 can only display graphics.
Note 2: DM1 and DM2 must be the same, regardless of the setting of W/S.

6-3-5-3 OV

Specifies two- or three-layer composition in graphics mode.
OV = 0: Two-layer composition
OV = 1: Three-layer composition

Set OV to 0 for mixed text and graphics mode.

6-3-6 CGRAM ADR

Specifies the CG RAM start address.

	MSB							LSB	
C	0	1	0	1	1	1	0	0	
P1	A7	A6	A5	A4	A3	A2	A1	A0	SAGL
P2	A15	A14	A13	A12	A11	A10	A9	A8	SAGH

Figure 6-19: CGRAM ADR Parameters

Note: See section 10 for information on the SAG parameters.

6-3-7 HDOT SCR

While the SCROLL command only allows scrolling by characters, HDOT SCR allows the screen to be scrolled horizontally by pixels. HDOT SCR cannot be used on individual layers.

	MSB							LSB
C	0	1	0	1	1	0	1	0
P1	0	0	0	0	0	D2	D1	D0

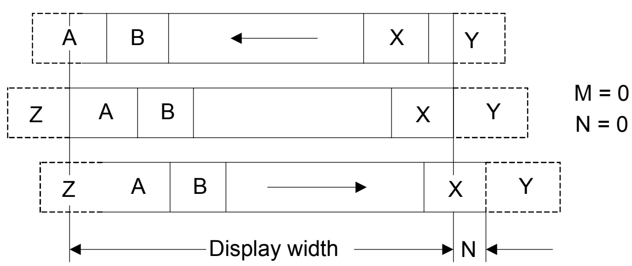
Figure 6-20: HDOT SCR Parameters

6-3-7-1 D0 to D2

Specifies the number of pixels to scroll. The C/R parameter has to be set to one more than the number of horizontal characters before using HDOT SCR. Smooth scrolling can be simulated if the controlling microprocessor repeatedly issues the HDOT SCR command to the RA8835 series. See Section 9-5 for more information on scrolling the display.

Table-18: Scroll Step Selection

P1				Number of pixels to scroll
HEX	D2	D1	D0	
00	0	0	0	0
01	0	0	1	1
02	0	1	0	2
↓	↓	↓	↓	↓
06	1	1	0	6
07	1	1	1	7



M/N is the number of bits(dots) that parameter 1 (P1) is incremented/decremented by.

Figure 6-21 Horizontal Scrolling

6-4 Drawing Control Commands

6-4-1 CSRW

The 16-bit cursor address register contains the display memory address of the data at the cursor position as shown in Figure 6-22. Note that the microprocessor cannot directly access the display memory. The MREAD and MWRITE commands use the address in this register.

	MSB							LSB	
C	0	1	0	0	0	1	1	0	
P1	A7	A6	A5	A4	A3	A2	A1	A0	(CSRL)
P2	A15	A14	A13	A12	A11	A10	A9	A8	(CSRH)

Figure 6-22: CSRW Parameters

The cursor address register can only be modified by the CSRW command, and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling. If a new address is not set, display memory accesses will be from the last set address or the address after previous automatic increments.

6-4-2 CSRR

Read from the cursor address register. After issuing the command, the data read address is read twice, for the low byte and then the high byte of the register.

	MSB							LSB	
C	0	1	0	0	0	1	1	1	
P1	A7	A6	A5	A4	A3	A2	A1	A0	(CSRL)
P2	A15	A14	A13	A12	A11	A10	A9	A8	(CSRH)

Figure 6-23: CSRR Parameters

6-5 Memory Control Commands

6-5-1 MWRITE

The microprocessor may write a sequence of data bytes to display memory by issuing the MREAD command and then writing the bytes to the RA8835 series. There is no need for further MWRITE commands or for the microprocessor to update the cursor address register after each byte as the cursor address is automatically incremented by the amount set with CSRDIR, in preparation for the next data write.

	MSB							LSB	
C	0	1	0	0	0	0	1	0	
P1									
P2									
...									
Pn									N≥1

Figure 6-24: MWRITE Parameters

Note: P1, P2, ..., Pn: display data.

6-5-2 MREAD

Put the RA8835 series into the data output state. Each time the microprocessor reads the buffer, the cursor address is incremented by the amount set by CSRDIR and the next data byte fetched from memory, so a sequence of data bytes may be read without further MREAD commands or by updating the cursor address register. If the cursor is displayed, the read data will be from two positions ahead of the cursor.

	MSB							LSB	
C	0	1	0	0	0	0	1	1	
P1									
P2									
...									
Pn									N≥1

Figure 6-25: MREAD Parameters

7. Functions Description

7-1 MCU Bus Interface

SEL1, SEL2, A0, $\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{CS}}$ are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the system address bus. SEL1 and SEL2 change the operation of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins to enable interfacing to either an 8080 or 6800 family bus, and should have a pull-up or pull-down resistor. With microprocessors using an 8080 family interface, the RA8835 series is normally mapped into the I/O address space.

7-1-1 8080 Series

Table-19: 8080 Series Interface Signals

A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	Function
0	0	1	Status flag read
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

7-1-2 6800 Series

Table-20A: 6800 Series Interface Signals

A0	R/$\overline{\text{W}}$	E	Function
0	1	1	Status flag read
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

7-2 MCU Synchronization

The RA8835 series interface operates at full bus speed, completing the execution of each command within the cycle time, t_{CYC}. The controlling microprocessor's performance is thus not hampered by polling or handshaking when accessing the RA8835 series.
Display flicker may occur if there is more than one consecutive access that cannot be ignored within a frame. The microprocessor can minimize this either by performing these accesses intermittently, or by continuously checking the status flag (D6) and waiting for it to become HIGH.

7-2-1 Display Status Indication Output

When $\overline{\text{CS}}$, A0 and $\overline{\text{RD}}$ are LOW, D6 functions as the display status indication output. It is HIGH during the TV-mode vertical retrace period or the LCD-mode horizontal retrace period, and LOW, during the period the controller is writing to the display. By monitoring D6 and writing to the data memory only during retrace periods, the display can be updated without causing screen flicker.

7-2-2 Internal Register Access

The SYSTEM SET and SLEEP IN commands can be used to perform input/output to the RA8835 series independently of the system clock frequency. These are the only commands that can be used while the RA8835 series is in sleep mode.

7-2-3 Display Memory Access

The RA8835 series supports a form of pipelined processing, in which the microprocessor synchronizes its processing to the RA8835 series timing. When writing, the microprocessor first issues the MWRITE command. It then repeatedly writes display data to the RA8835 series using the system bus timing. This ensures that the microprocessor is not slowed down even if the display memory access times are slower than the system bus access times. See Figure 7-1A.

When reading, the microprocessor first issues the MREAD command, which causes the RA8835 series to load the first read data into its output buffer. The microprocessor then reads data from the RA8835 series using the system bus timing. With each read, the RA8835 series reads the next data item from the display memory ready for the next read access. See Figure 7-1B.

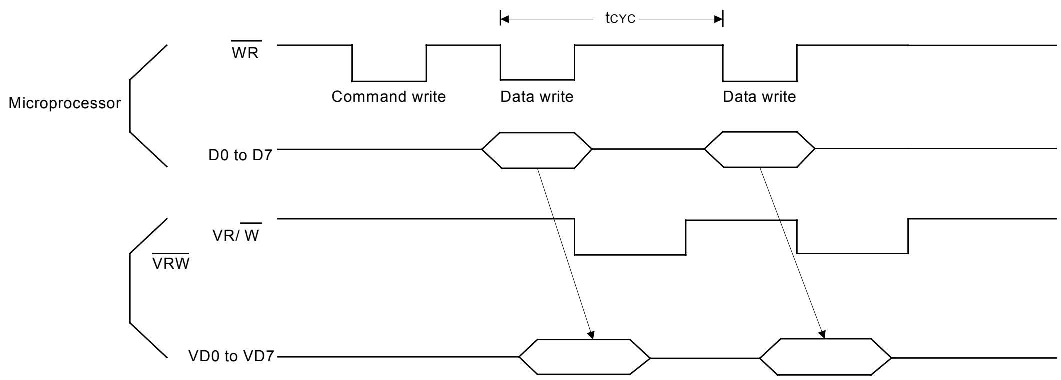


Figure 7-1A: Display Memory Write Cycle

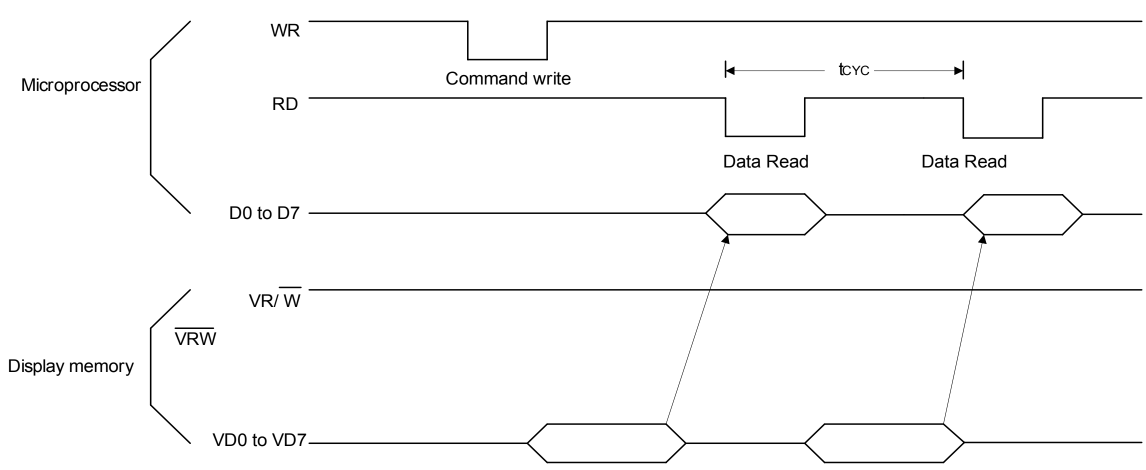


Figure 7-1B: Display Memory Read Cycle

Note: A possible problem with the display memory read cycle is that the system bus access time, t_{ACC}, does not depend on the display memory access time, t_{ACV}. The microprocessor may only make repeated reads if the read loop time exceeds the RA8835 series cycle time, t_{CYC}. If it does not, NOP instructions may be inserted in the program loop. t_{ACC}, t_{ACV} and t_{CYC} limits

are given in section 7-2.

7-3 MCU Interface Examples

7-3-1 Z80 to RA8835 Interface

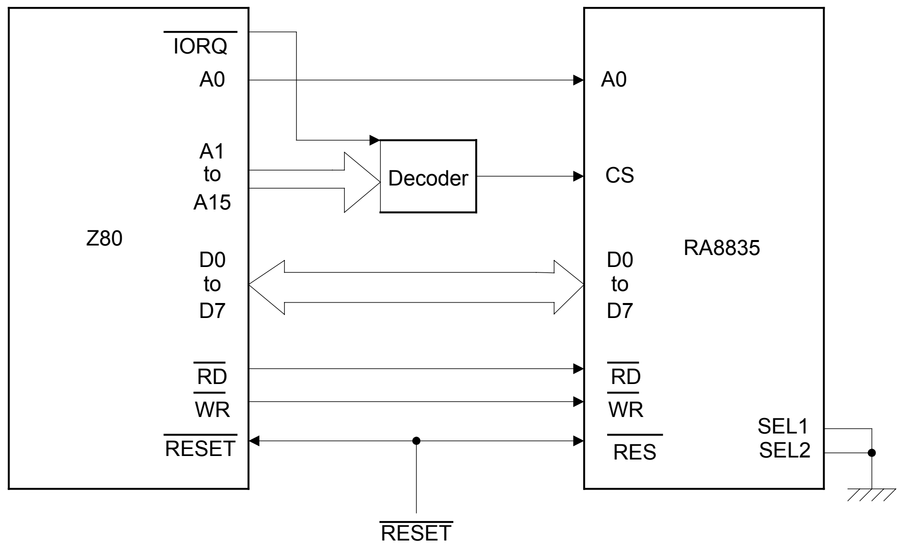


Figure 7-2A: Z80 to RA8835 Interface

7-3-2 6802 to RA8835 Interface

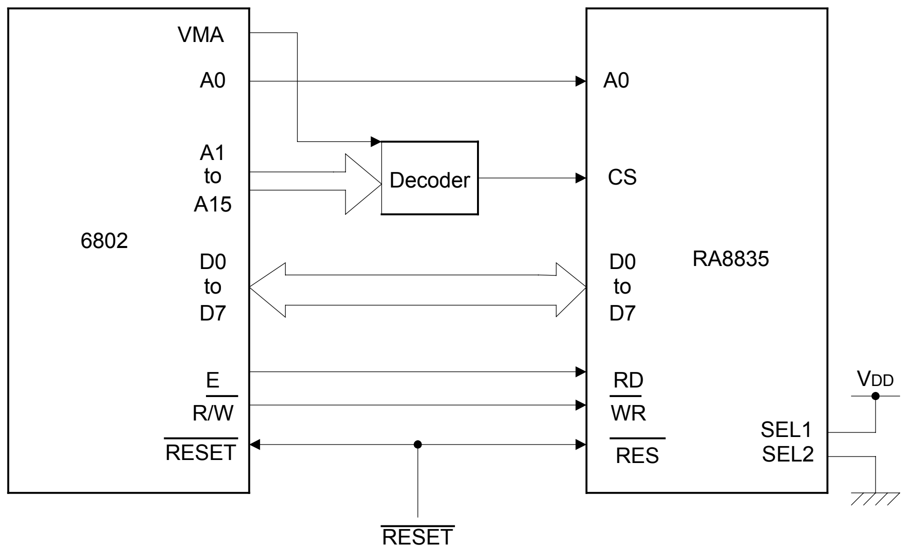


Figure 7-2B: 6802 to RA8835 Interface

7-4 Static RAM

The figure below shows the interface between an 8Kx8 static RAM and the RA8835 series. Note that bus buffers are required if the bus is heavily loaded.

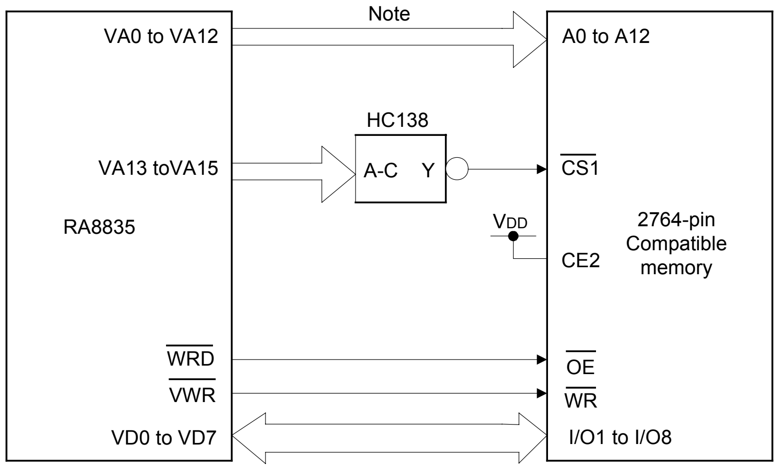


Figure 7-3: Static RAM Interface

Note: If the bus loading is too much, use a bus buffer.

7-5 Supply Current during Display Memory Access

The 24 address and data lines of the RA8835 series cycle at one-third of the oscillator frequency, f_{OSC}. The charge and discharge current on these pins, I_{VOP}, is given by the equation below. When I_{VOP} exceeds I_{OPR}, it can be estimated by:

$$IVOP \propto C\,V\,f$$

Where C is the capacitance of the display memory bus, V is the operating voltage, and f is the operating frequency. If V_{OPR} = 5.0V, f = 1.0 MHz, and the display memory bus capacitance is 1.0 pF per line:

$$I_{VOP} \leq 120\ mA / MHz \times pF$$

To reduce current flow during display memory accesses, it is important to use low-power memory, and to minimize both the number of devices and the parasitic capacitance.

7-6 Oscillator Circuit

The RA8835 series incorporates an oscillator circuit. A stable oscillator can be constructed simply by connecting an AT-cut crystal and two capacitors to XG and XD, as shown in the figure below. If the oscillator frequency is increased, CD and CG should be decreased proportionally. Note that the circuit board lines to XG and XD must be as short as possible to prevent wiring capacitance from changing the oscillator frequency or increasing the power consumption.

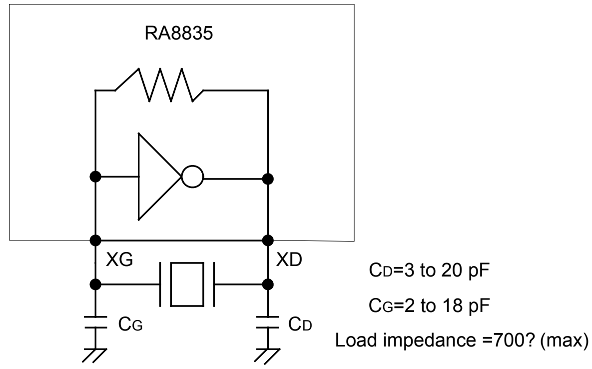


Figure 7-4: Crystal Oscillator

7-7 Status Flag

The RA8835 series has a single bit status flag.
D6: X line standby

D7							D0
X	D6	X	X	X	X	X	X

X:Don't care

Figure 7-5: Status Flag

The D6 status flag is HIGH for the TC/R-C/R cycles at the end of each line where the RA8835 series is not reading the display memory. The microprocessor may use this period to update display memory without affecting the display, however it is recommended that the display be turned off when refreshing the whole display.

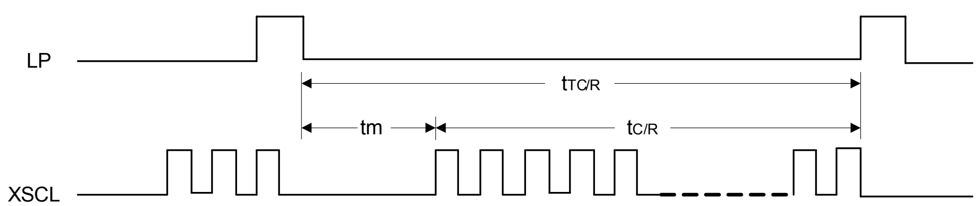


Figure 7-6: C/R to TC/R Time Difference

$\overline{CS}$	A0	$\overline{RD}$	D_6(flag)
0	0	0	0: Period of retrace lines
0	0	0	1: Period of display

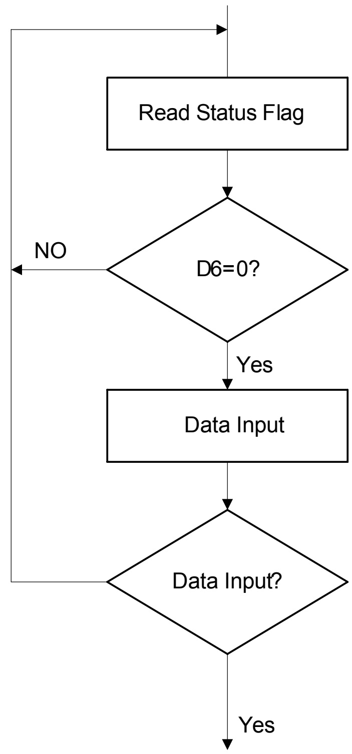
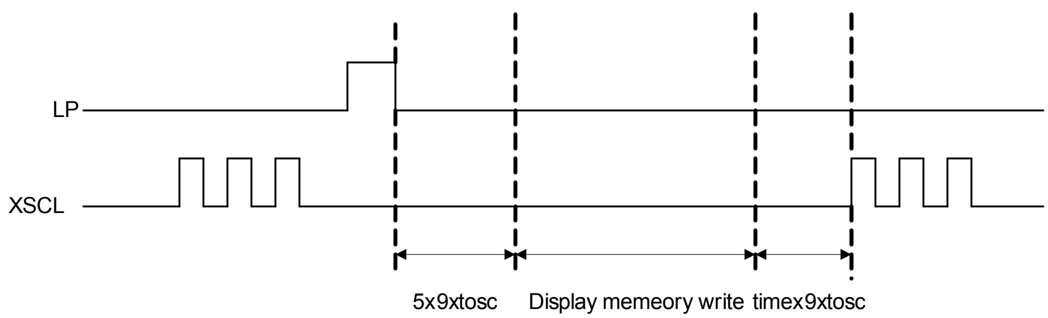


Figure 7-7: Flowchart for Busy Flag Checking

- **Precaution on the write timing to VRAM**



The allowable writing duration is since "5 x 9 x t_{OSC}" has elapsed (t_{OSC} = 1/f_{OSC}: a cycle of the oscillation frequency) from the positive going edge of LP up to {(TCR) – (C/R) – 7} x 9 x t_{OSC}.

Currently employed D6 status flag reading method does not identify the timing when the read D6 = Low took place. Thus, negative going edge of LP should be used as the interrupt signal when implementing the writing in above timing. If you try to access the display memory in other timing than the above, flickering of the display screen will result.

7-8 Reset

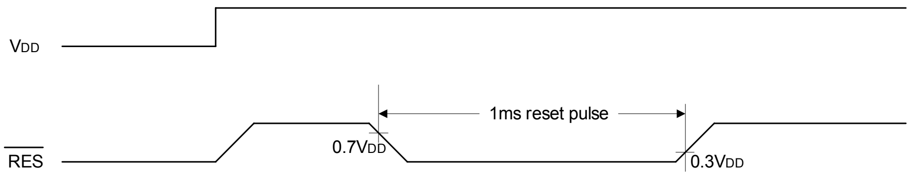


Figure 7-8: Reset Timing

The RA8835 series requires a reset pulse at least 1 ms long after power-on in order to re-initialize its internal state. For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the RA8835 series is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse.

The RA8835 series cannot receive commands while it is reset. Commands to initialize the internal registers should be issued soon after a reset. During reset, the LCD drive signals XD, LP and FR are halted. A delay of 3 ms (maximum) is required following the rising edges of both RES and VDD to allow for system stabilization.

7-9 Character Configuration

The origin of each character bitmap is in the top left corner as shown in Figure 7-9. Adjacent bits in each byte are horizontally adjacent in the corresponding character image. Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.

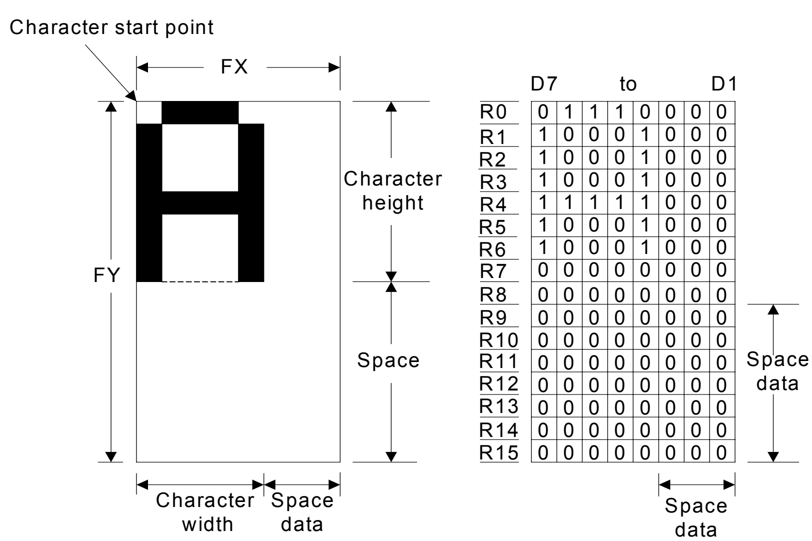


Figure 7-9: Example of Character Display ([FX] $\leq$ 8) and Generator Bitmap

If the area outside the character bitmap contains only zeros, the displayed character size can easily be increased by increasing FX and FY, as the zeros ensure that the extra space between displayed characters is blank. The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.

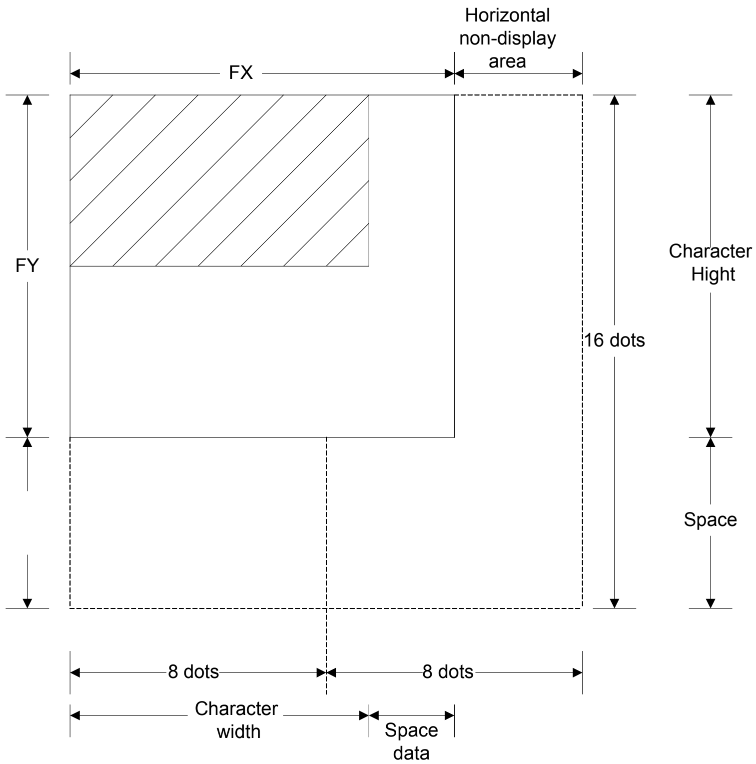


Figure 7-10: Character Width Greater Than One Byte Wide ([FX]=9)

Note: The RA8835 series does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row, even though the character image requires only one.

7-10 Screen Configuration

7-10-1 Screen Configuration

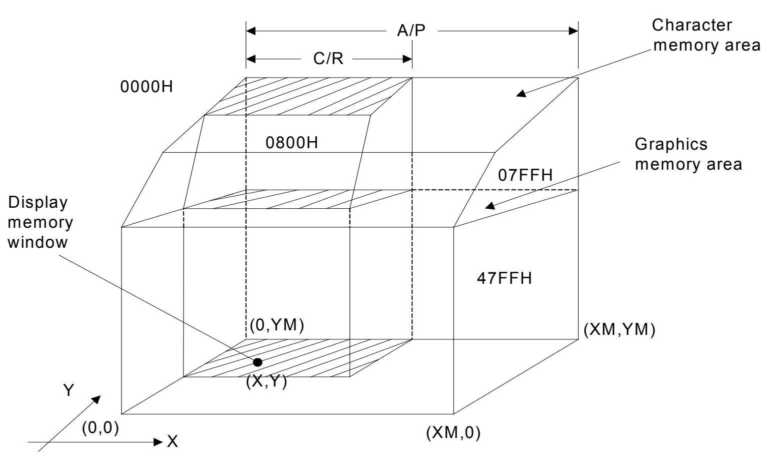


Figure 7-11: Virtual and Physical Screen Relationship

The basic screen configuration of the RA8835 series is as a single text screen or as overlapping text and graphics screens. The graphics screen uses eight times as much display memory as the text screen. Figure 7-11 shows the relationship between the virtual screens and the physical screen.

7-10-2 Display Address Scanning

The RA8835 series scans the display memory in the same way as a raster scan CRT screen. Each row is scanned from left to right until the address range equals C/R. Rows are scanned from top to bottom.
In graphics mode, at the start of each line, the address counter is set to the address at the start of the previous line plus the address pitch, AP.

In text mode, the address counter is set to the same start address, and the same character data is read, for each row in the character bitmap. However, a new row of the character generator output is used each time. Once all the rows in the character bitmap have been displayed, the address counter is set to the start address plus AP and the next line of text is displayed.

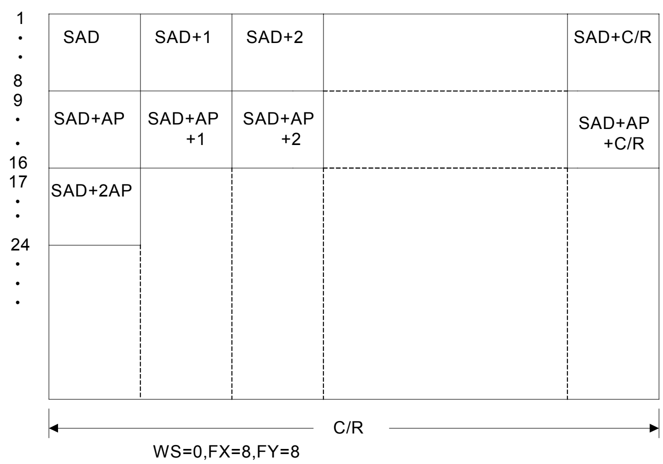


Figure 7-12: Character Position Parameters

Note: One byte of display memory corresponds to one character.

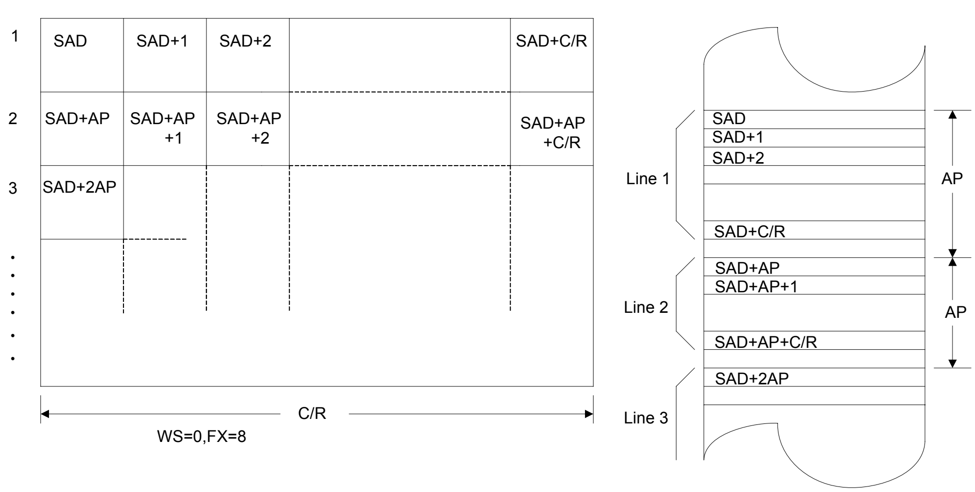


Figure 7-13: Character Parameters vs. Memory

Note: One bit of display memory corresponds to one pixel.

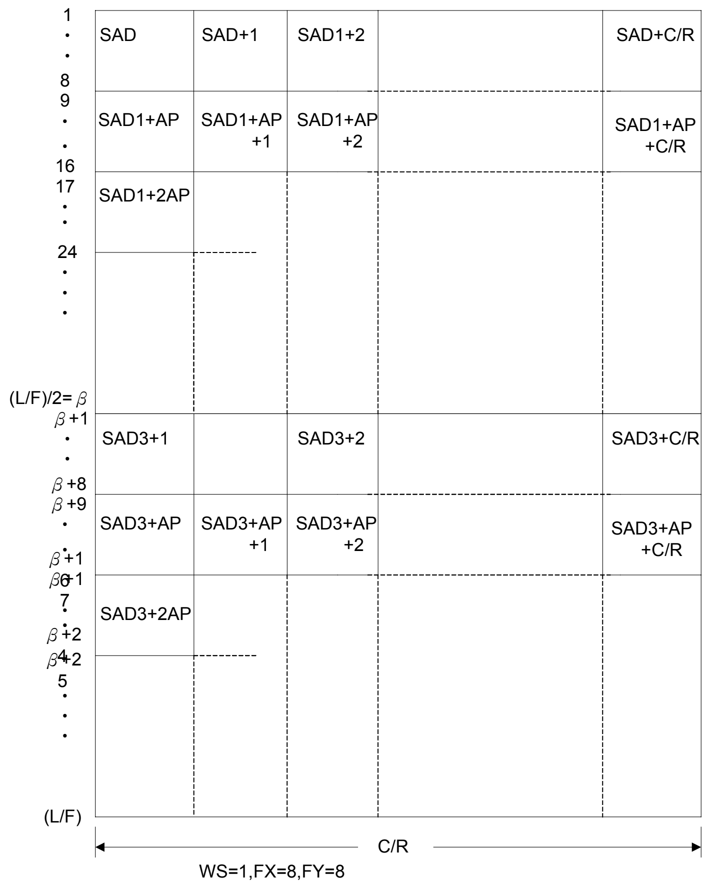


Figure 7-14: Two-panel Display Address Indexing

Note: In two-panel drive, the RA8835 series reads line 1 and line b + 1 as one cycle. The upper and lower panels are thus read alternately, one line at a time.

7-10-3 Display Scan Timing

Figure 7-15 shows the basic timing of the RA8835 series. One display memory read cycle takes nine periods of the system clock, $\phi 0$ (f_{OSC}). This cycle repeats (C/R + 1) times per display line. When reading, the display memory pauses at the end of each line for (TC/R - C/R) display memory read cycles, though the LCD drive signals are still generated. TC/R may be set to any value within the constraints imposed by C/R, f_{OSC} , f_{FR} , and the size of the LCD panel, and it may be used to fine tune the frame frequency. The microprocessor may also use this pause to access the display memory data.

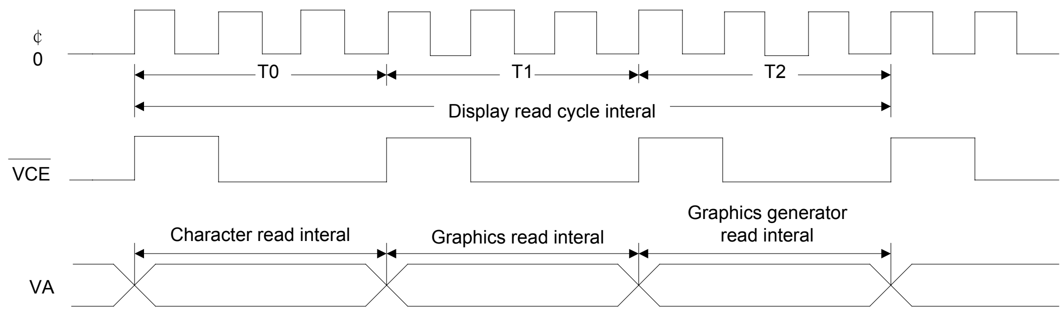


Figure 7-15: Display Memory Basic Read Cycle

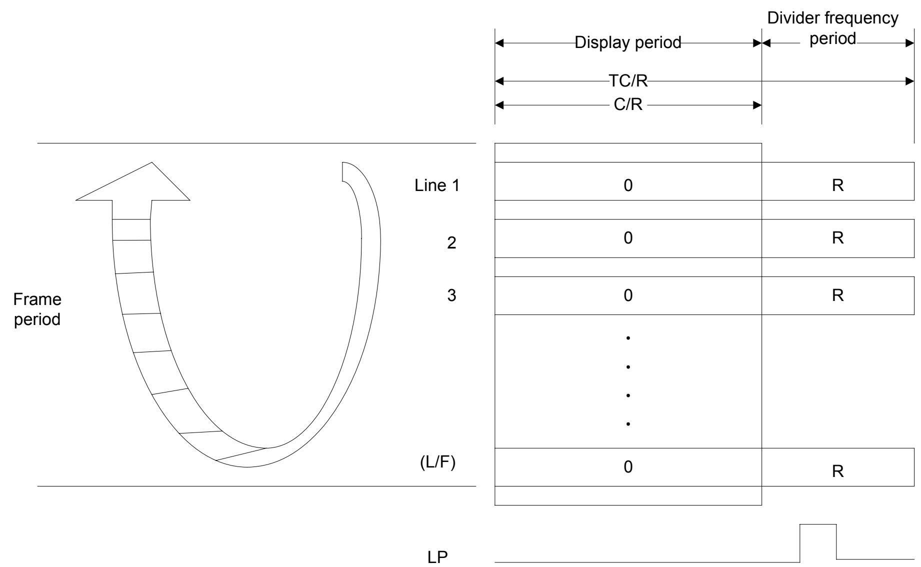


Figure 7-16: Relationship Between TC/R and C/R

Note: The divider adjustment interval (R) applies to both the upper only at the end of the lower screen's display interval.

7-11 Cursor Control

7-11-1 Cursor Register Function

The RA8835 series cursor address register functions as both the displayed cursor position address register and the display memory access address register. When accessing display memory outside the actual screen memory, the address register must be saved before accessing the memory and restored after memory access is complete.

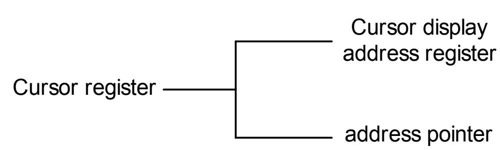


Figure 7-17: Cursor Addressing

Note that the cursor may disappear from the display if the cursor address remains outside the displayed screen memory for more than a few hundred milliseconds.

7-11-2 Cursor Movement

On each memory access, the cursor address register changes by the amount previously specified with CSRDIR, automatically moving the cursor to the desired location.

7-11-3 Cursor Display Layers

Although the RA8835 series can display up to three layers, the cursor is displayed in only one of these layers: Two-layer configuration: First layer (L1) Three-layer configuration: Third layer (L3) The cursor will not be displayed if it is moved outside the memory for its layer. Layers may be swapped or the cursor layer moved within the display memory if it is necessary to display the cursor on a layer other than the present cursor layer.

Although the cursor is normally displayed for character data, the RA8835 series may also display a dummy cursor for graphical characters. This is only possible if the graphics screen is displayed, the text screen is turned off and the microprocessor generates the cursor control address.

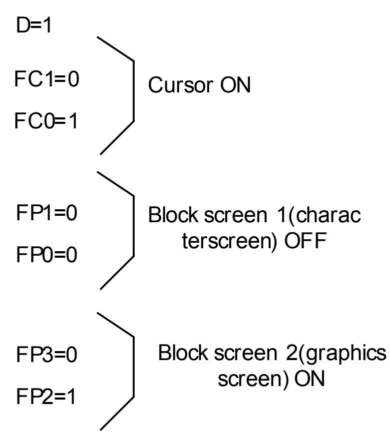


Figure 7-18: Cursor Display Layers

Consider the example of displaying Chinese characters on a graphics screen. To write the display data, the cursor address is set to the second screen block, but the cursor is not displayed. To display the cursor, the cursor address is set to an address within the blank text screen block. Since the automatic cursor increment is in address units, not character units, the controlling microprocessor must set the cursor address register when moving the cursor over the graphical characters.

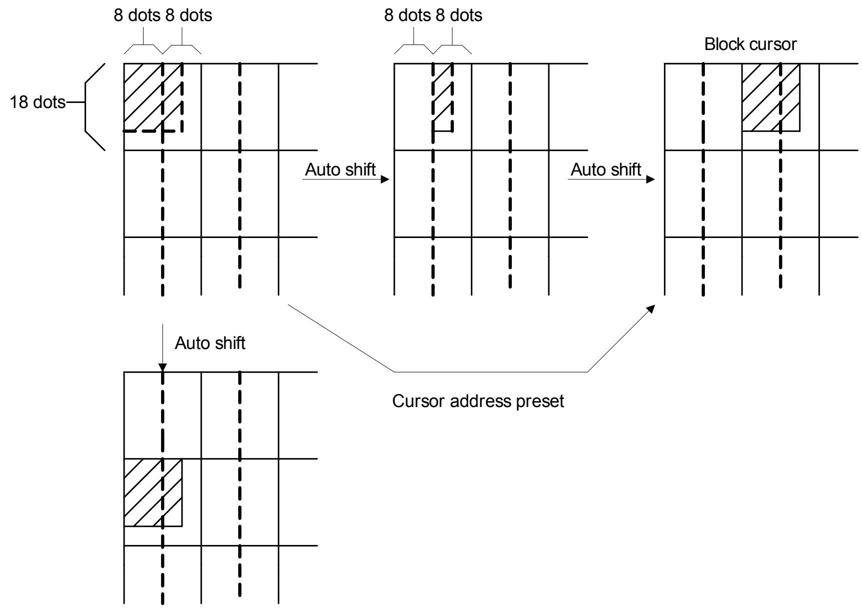


Figure 7-19: Cursor Movement

If no text screen is displayed, only a bar cursor can be displayed at the cursor address.
If the first layer is a mixed text and graphics screen and the cursor shape is set to a block cursor, the RA8835 series automatically decides which cursor shape to display. On the text screen it displays a block cursor, and on the graphics screen, a bar cursor.

7-12 Memory to Display Relationship

The RA8835 series supports virtual screens that are larger than the physical size of the LCD panel address range, C/R. A layer of the RA8835 series can be considered as a window in the larger virtual screen held in display memory. This window can be divided into two blocks, with each block able to display a different portion of the virtual screen.

This enables, for example, one block to dynamically scroll through a data area while the other acts as a status message display area. See Figure 7-20 and 7-21.

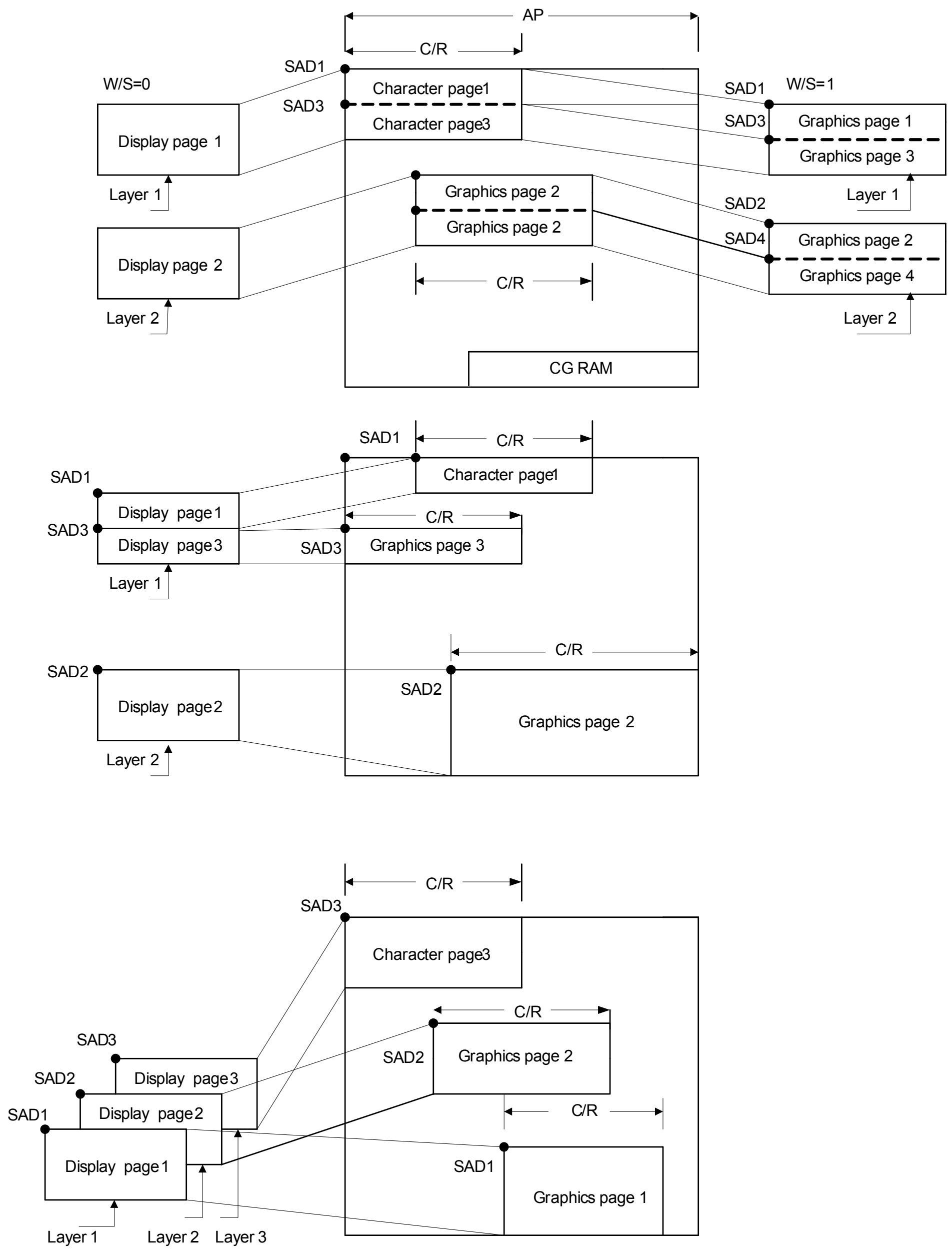


Figure 7-20: Display Layers and Memory

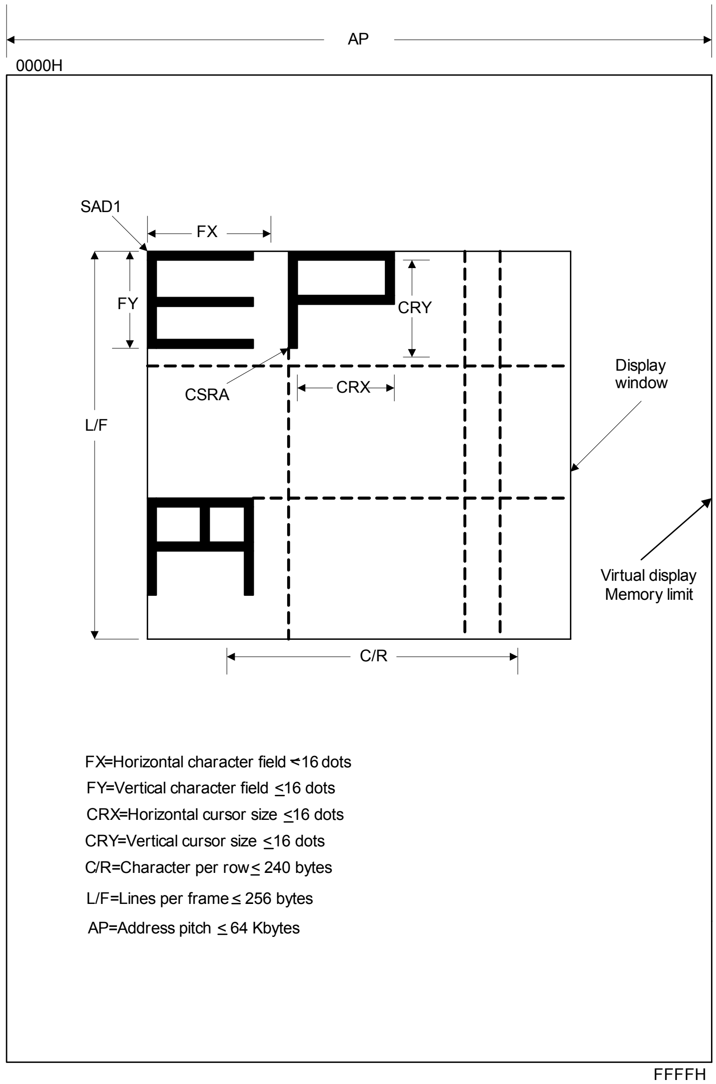


Figure 7-21: Display Windows and Memory

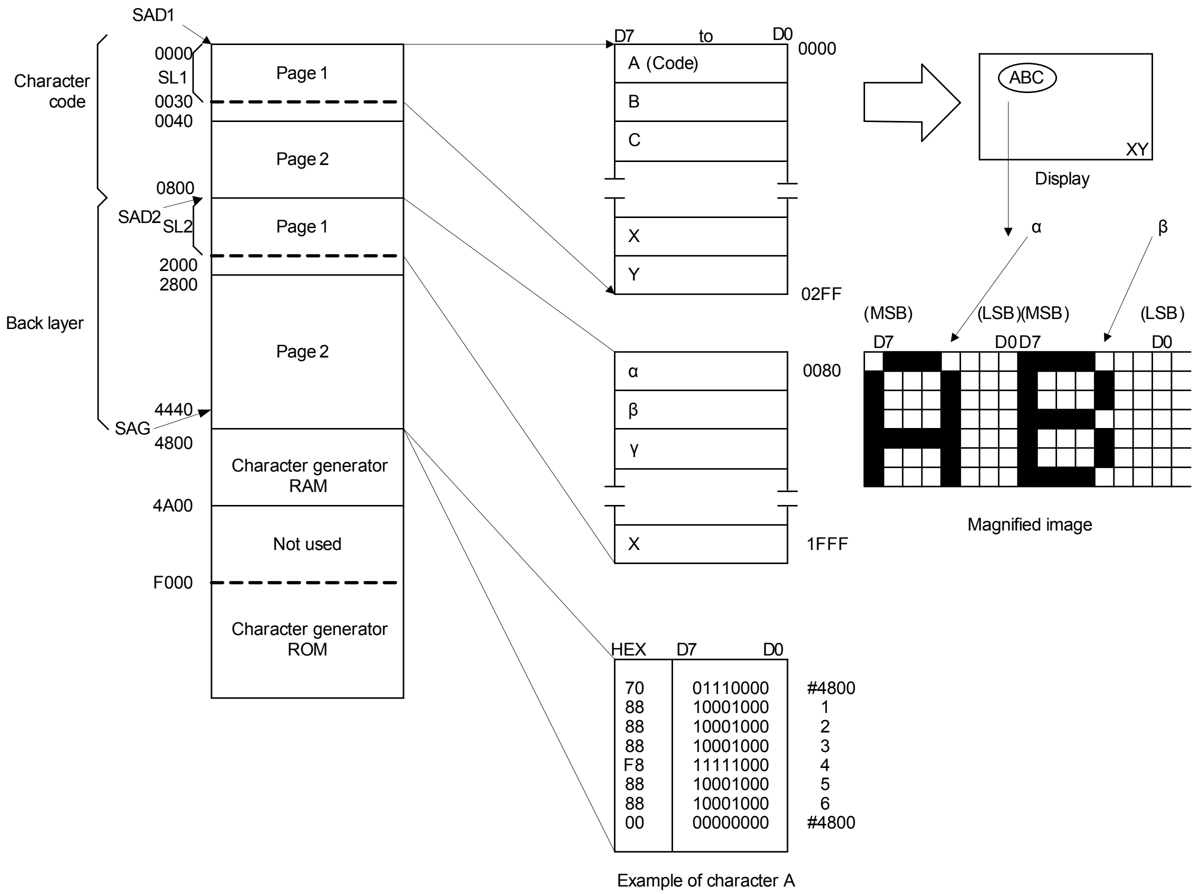


Figure 7-22: Memory Map and Magnified Characters

7-13 Scrolling

The controlling microprocessor can set the RA8835 series scrolling modes by overwriting the scroll address registers SAD1 to SAD4, and by directly setting the scrolling mode and scrolling rate.

7-13-1 On-page Scrolling

The normal method of scrolling within a page is to move the whole display up one line and erase the bottom line. Since the RA8835 series does not automatically erase the bottom line, it must be erased with blanking data when changing the scroll address register.

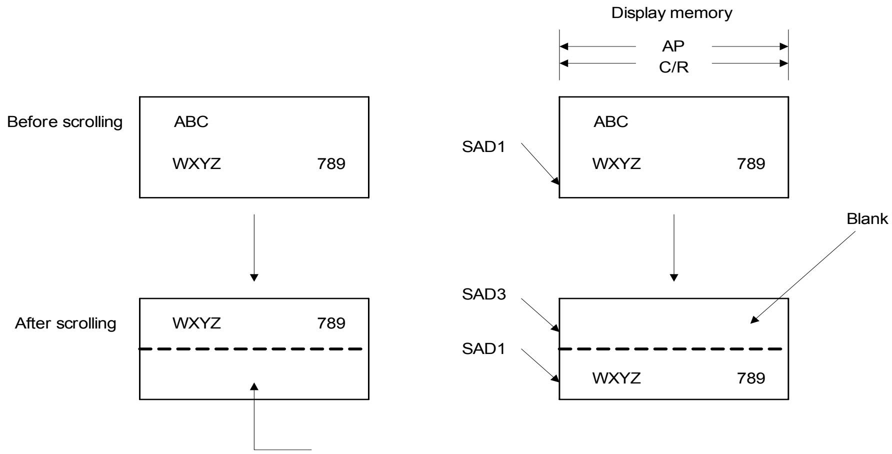


Figure 7-23: On-page Scrolling

7-13-2 Inter-page Scrolling

Scrolling between pages and page switching can be performed only if the display memory capacity is greater than one screen.

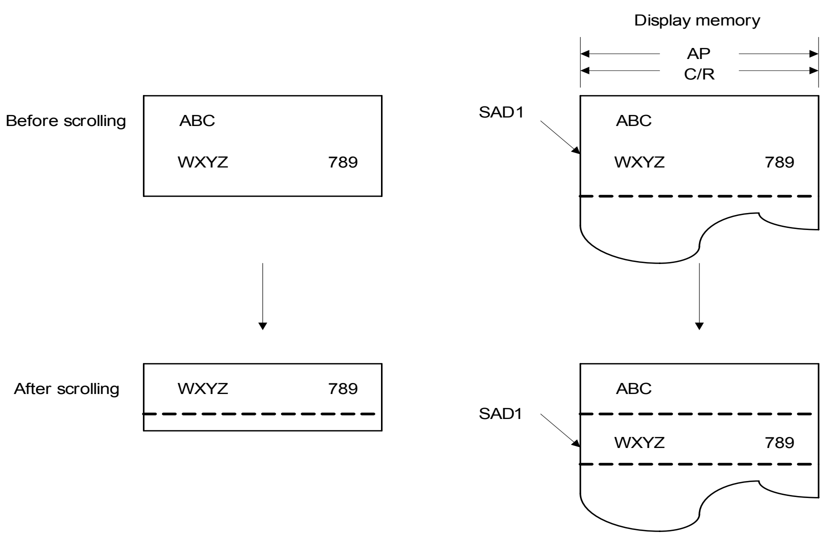


Figure 7-24: Inter-page Scrolling

7-13-3 Horizontal Scrolling

The display can be scrolled horizontally in one-character units, regardless of the display memory capacity.

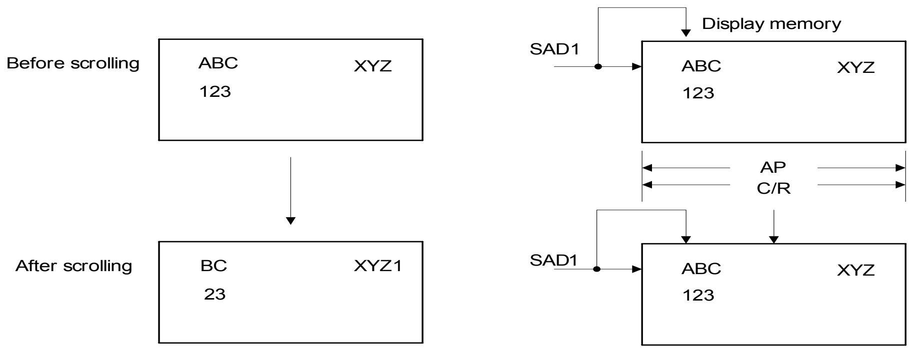


Figure 7-25: Horizontal Wraparound Scrolling

7-13-4 Bi-directional Scrolling

Bi-directional scrolling can be performed only if the display memory is larger than the physical screen both horizontally and vertically. Although scrolling is normally done in single-character units, the HDOT SCR command can be used to scroll horizontally in pixel units. The Single-pixel scrolling of both horizontally and vertically can be performed by using the SCROLL and HDOT SCR commands. See Section 17-4.

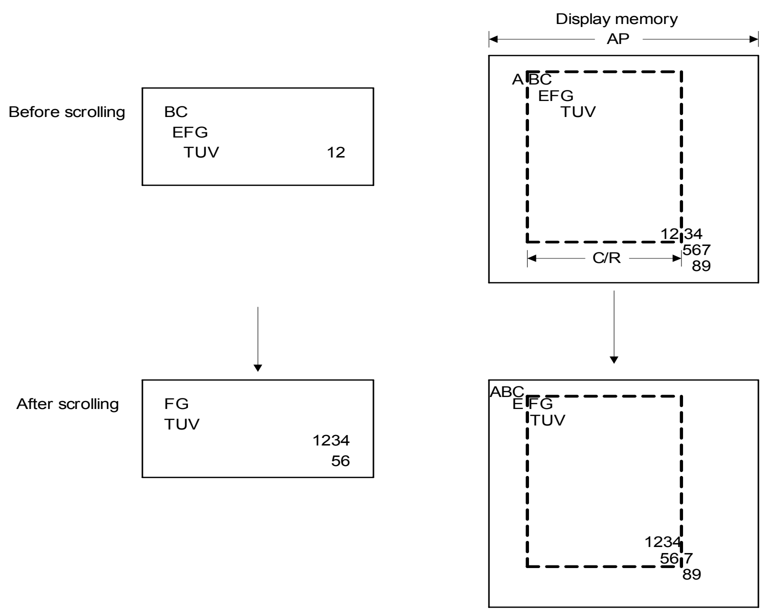


Figure 7-26: Bi-directional Scrolling

7-13-5 Scroll Units

Table-20B: Scroll Units

Mode	Vertical	Horizontal
Text	Characters	Pixels or characters
Graphics	Pixels	Pixels

Note that in a divided screen, each block cannot be independently scrolled horizontally in pixel units.

7-14 CG Characteristics

7-14-1 Internal Character Generator

The internal character generator is recommended for minimum system configurations containing a RA8835 series, display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator uses a CMOS mask ROM, it is also recommended for low-power applications.

- 5 x 7-pixel font (See Section 18.)
- 160 JIS standard characters
- Can be mixed with character generator RAM (maximum of 64 CG RAM characters)
- Can be automatically spaced out up to 8 x 16 pixels

7-14-2 External Character Generator ROM

The external CG ROM can be used when fonts other than those in the internal ROM are needed. Data is stored in the external ROM in the same format used in the internal ROM. (See Section 11-4)

- Up to 8 x 8-pixel characters (M2 = 0) or 8 x 16-pixel characters (M2 = 1)
- Up to 256 characters (192 if used together with the internal ROM)
- Mapped into the display memory address space at F000H to F7FFH (M2 = 0) or F000H to FFFFH (M2 = 1)
- Characters can be up to 8 x 16-pixels; however, excess bits must be set to zero.

7-14-3 Character Generator RAM

The user can freely use the character generator RAM for storing graphics characters. The character generator RAM can be mapped by the microprocessor anywhere in display memory, allowing effective use of unused address space.

- Up to 8 x 8-pixel characters (M2 = 0) or 8 x 16 characters (M2 = 1)
- Up to 256 characters if mapped at F000H to FFFFH (64 if used together with character generator ROM)
- Can be mapped anywhere in display memory address space if used with the character generator ROM
- Mapped into the display memory address space at F000H to F7FFH if not used with the character generator ROM (more than 64 characters are in the CG RAM). Set SAG0 to F000H and M1 to zero when defining characters number 193 upwards.

7-15 CG Memory Allocation

Since the RA8835 series uses 8-bit character codes, it can handle no more than 256 characters at a time. However, if a wider range of characters is required, character generator memory can be bank-switched using the CGRAM ADR command.

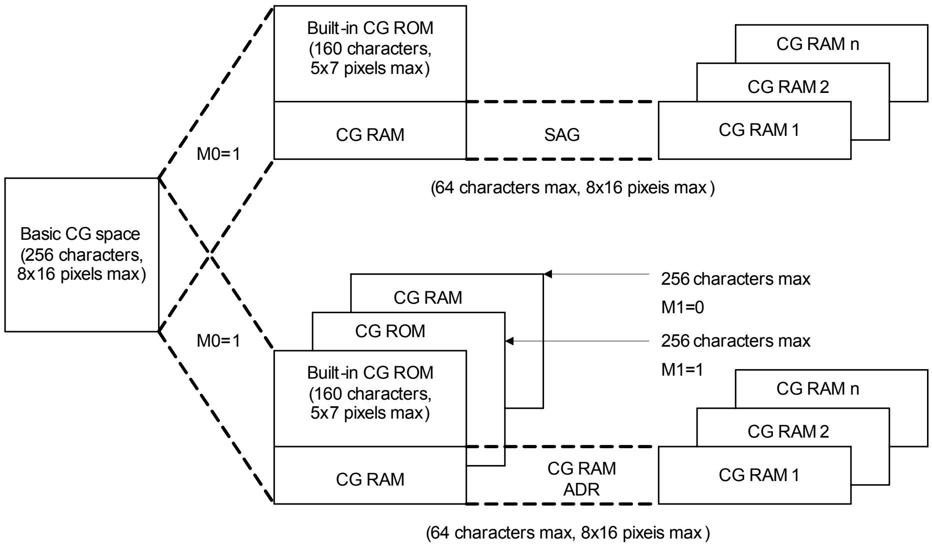


Figure 7-27: Internal and External Character Mapping

Note that there can be no more than 64 characters per bank.

Table-21: Character Mapping

Item		Parameter	Remarks
Internal/external character generator selection		M0	
Character field height	1 to 8 pixels	M2 = 0	
	9 to 16 pixels	M2 = 1	
	Greater than 16 pixels	Graphics mode (8 bits ´1 line)	
Internal CG ROM/RAM select External CG ROM/RAM select		Automatic	Determined by the character code
CG RAM bit 6 correction		M1	
CG RAM data storage address		Specified with CG RAM ADR command	Can be moved anywhere in the display memory address space
External CG ROM Address	192 characters or less	Other than the area of Figure 7-2A	
	More than 192 characters	Set SAG to F000H and overly SAG and the CG ROM table	

7-16 Setting Character Generator Address

The CG RAM addresses in the VRAM address space are not mapped directly from the address in the SAG register. The data to be displayed is at a CG RAM address calculated from SAG + character code + ROW select address. This mapping is shown in Table-22A and –22B.

Table-22A: Character Fonts, Number of Lines $\leq$ 8 (M2 = 0, M1 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ROW select	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0

address																
CG RAM address	VA 15	VA1 4	VA1 3	VA 12	VA1 1	VA1 0	VA 9	VA 8	VA 7	VA 6	VA 5	VA 4	VA 3	VA 2	VA 1	VA 0

Table-22B: Character Fonts, 9 ≤ Number of Lines ≤ 16 (M2 = 1, M1 = 0)

SAG	**A1 5**	**A1 4**	**A1 3**	**A1 2**	**A1 1**	**A1 0**	**A9**	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
Character code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ROW select address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CG RAM address	VA 15	VA1 4	VA1 3	VA 12	VA1 1	VA1 0	VA 9	VA 8	VA 7	VA 6	VA 5	VA 4	VA 3	VA 2	VA 1	VA 0

ROW	R3	R2	R1	R0
ROW 0	0	0	0	0
ROW 1	0	0	0	1
ROW 2	0	0	1	0
↓	↓	↓	↓	↓
ROW 7	0	1	1	1
ROW 8	1	0	0	0
↓	↓	↓	↓	↓
ROW 14	1	1	1	0
ROW 15	1	1	1	1

Line 1 (ROW 0 – ROW 7)
Line 2 (ROW 0 – ROW 15)

Figure 7-28: Row Select Address

Note: Lines = 1: lines in the character bitmap ≤ 8
Lines = 2: lines in the character bitmap ≤ 9

7-16-1 M1 = 1

The RA8835 series automatically converts all bits set in bit 6 of character code for CG RAM 2 to zero. Because of this, the CG RAM data areas become contiguous in display memory.
When writing data to CG RAM:

- Calculate the address as for M1 = 0.
- Change bit 6 of the character code from “1” to “0”.

7-16-2 CG RAM Addressing Example

- Define a pattern for the “A” in Figure 7-9.
- The CG RAM table start address is 4800H.
- The character code for the defined pattern is 80H (the first character code in the CG RAM area).

As the character code table in Figure 7-29 shows, codes 80H to 9FH and E0H to FFH are

allocated to the CG RAM and can be used as desired. 80H is thus the first code for CG RAM. As characters cannot be used if only using graphics mode, there is no need to set the CG RAM data.

Table-23: Character Data Example

CGRAM AD	5CH	Reverse the CG RAM address calculation to calculate SAG
P1	00H	
P2	40H	
CSRDIR	4CH	Set cursor shift direction to right
CSRW	46H	CG RAM start address is 4800H
P1	00H	
P2	48H	
MWRITE	42H	
P	70H	Write ROW 0 data
P2	88H	Write ROW 1 data
P3	88H	Write ROW 2 data
P4	88H	Write ROW 3 data
P5	F8H	Write ROW 4 data
P6	88H	Write ROW 5 data
P7	88H	Write ROW 6 data
P8	00H	Write ROW 7 data
P8	00H	Write ROW 8 data
↓	↓	↓
P16	00H	Write ROW 15 data

7-17 Character Codes

The following figure shows the character codes and the codes allocated to CG RAM. The CG RAM if not using the internal ROM can use all codes.

	Upper 4bites															
Lower 4bites	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0				0	@	P	‘	p								
1			!	1	A	Q	a	q								
2			“	2	B	R	b	r								
3			#	3	C	S	c	s								
4			$	4	D	T	d	t								
5			&	5	E	U	e	u								
6			%	6	F	V	f	v								
7			'	7	G	W	g	w								
8			(	8	H	X	h	x								
9			)	9	I	Y	i	y								
A			*	:	J	Z	j	z								
B			+	;	K	[	k	{								
C			,	<	L	¥	l	¦								
D			·	=	M	]	m	}								
E			-	>	N	^	n	→								
F			/	?	O	_	o	←								

CG RAM 1 (columns 8–9)
CG RAM2 (columns E–F)
M1=0
M1=1

Figure 7-29: On-chip Character Codes

8. Application Notes

8-1 Initialization Parameters

The parameters for the initialization commands must be determined first. Square brackets around a parameter name indicate the number represented by the parameter, rather than the value written to the parameter register. For example, [FX] = FX + 1.

8-1-1 SYSTEM SET Instruction and Parameters

◎ FX

The horizontal character field size is determined from the horizontal display size in pixels [VD] and the number of characters per line [VC].

$$\frac{[VD]}{[VC]} \leq [FX]$$

◎ C/R

C/R can be determined from VC and FX.

$$[C/R] = RND(\frac{[FX]}{8}) \times [VC]$$

Where RND(x) denotes ´ rounded up to the next highest integer. [C/R] is the number of bytes per line, not the number of characters.

◎ TC/R

TC/R must satisfy the condition $[TC/R] \geq [C/R] + 4$.

◎ f_{OSC} and f_{FR}

Once TC/R has been set, the frame frequency, f_{FR}, and lines per frame [L/F] will also have been set. The lower limit on the oscillator frequency f_{OSC} is given by:

$$f_{OSC} \geq ([TC/R] \times 9 + 1) \times [L/F] \times f_{FR}$$

◎ If no standard crystal close to the calculated value of f_{OSC} exists, a higher frequency crystal can be used and the value of TC/R revised using the above equation.

◎ Symptoms of an incorrect TC/R setting are listed below. If any of these appears, check the value of TC/R and modify it if necessary.

- Vertical scanning halts and a high-contrast horizontal line appears.
- All pixels are on or off.
- The LP output signal is absent or corrupted.
- The display is unstable.

Table-24: RAiO LCD Unit Example Parameters

Product name and resolution (X ´Y)	[FX]	[FY]	[C/R]	TC/R	f_{OSC} (MHz) See Note 2.
256 x 64	[FX] = 6 pixels: 256 / 6 = 42 remainder 4 = 4 blank pixels	8 or 16, depending on the screen	[C/R] = 42 = 2AH bytes: C/R = 29H. When using HDOT SCR, [C/R] = 43 bytes	2DH	1.85
512 x 64	[FX] = 6 pixels: 512 / 6 = 85	8 or 16, depending on the screen	[C/R] = 85 = 55H bytes:	58H	3.59

	remainder 2 = 2 blank pixels		C/R = 54H. When using HDOT SCR, [C/R] = 86 bytes		
256 x 128	[FX] = 8 pixels: 256 / 8 = 32 remainder 0 = no blank pixels	8 or 16, depending on the screen	[C/R] = 32 = 20H bytes: C/R = 19H. When using HDOT SCR, [C/R] = 33 bytes	22H	2.90
512 x 128	[FX] = 10 pixels: 512 / 10 = 51 remainder 2 = 2 blank pixels	8 or 16, depending on the screen	[C/R] = 102 = 66H bytes: C/R = 65H. When using HDOT SCR, [C/R] = 103 bytes	69H	8.55

Notes:
1. The remainder pixels on the right-hand side of the display are automatically blanked by the RA8835. There is no need to zero the display memory corresponding to these pixels.
2. Assuming a frame frequency of 60 Hz.

8-1-2 Initialization Example

The initialization example shown in Figure 8-1 is for a RA8835 series with an 8-bit microprocessor interface bus and a display unit (320 x 240 pixels).

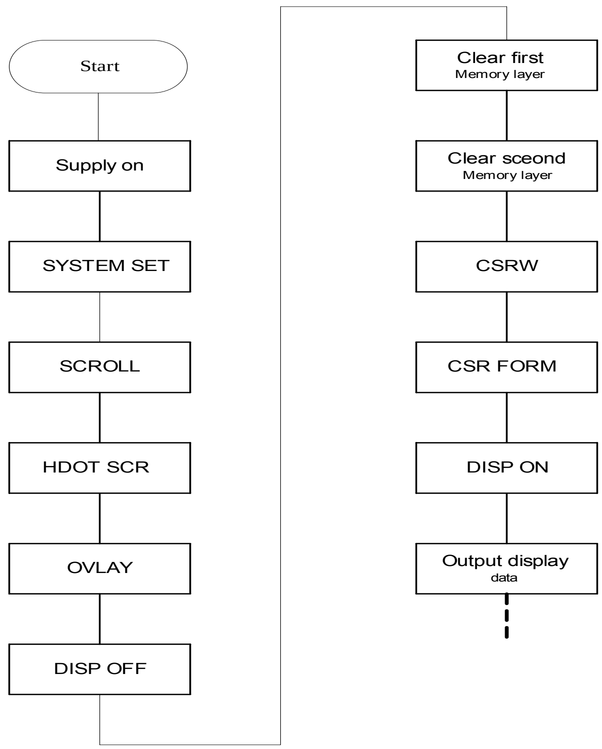
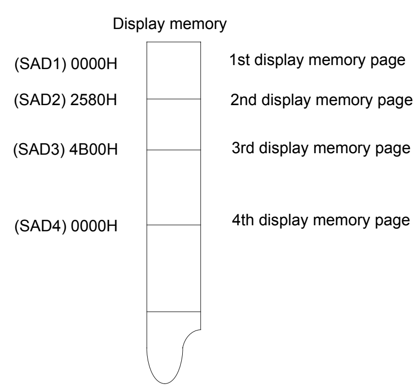


Figure 8-1: Initialization Procedure

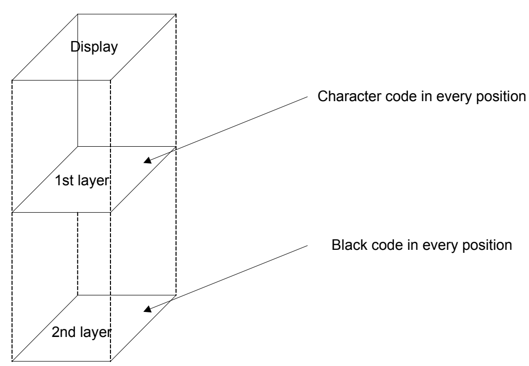
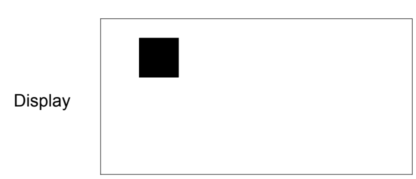
Note: Set the cursor address to the start of each screen's layer memory, and use MWRITE to fill the memory with space characters, 20H (text screen only) or 00H (graphics screen only). Determining which memory to clear is explained in section 17-1-3.

Table-25: Initialization Procedure

No.	Command	Operation
1	Power-up	
2	Supply	
3	SYSTEM SET	
	C = 40H	
	P1 = 30H	M0: Internal CG ROM M1: CG RAM is 32 characters maximum M2: 8 lines per character W/S: Two-panel drive IV: No top-line compensation
	P2 = 87H	FX: Horizontal character size = 8 pixels WF: Two-frame AC drive
	P3 = 07H	FY: Vertical character size = 8 pixels
	P4 = 27H	C/R: 39 display addresses per line
	P5 = 2FH	TC/R: Total address range per line = 47 f_{OSC} = 8.0 MHz, f_{FR} = 70 Hz
	P6 = EFH	L/F: 239 display lines
	P7 = 28H	AP: Virtual screen horizontal size is 40 addresses
	P8 = 00H	
4	SCROLL	
	C = 44H	
	P1 = 00H	First screen block start address
	P2 = 00H	Set to 0000H
	P3 = F0H	Display lines in first screen block = 240
	P4 = 80H	Second screen block start address
	P5 = 25H	Set to 1000H
	P6 = F0H	Display lines in second screen block = 240
	P7 = 00H	Third screen block start address
	P8 = 4BH	Set to 4B00H
	P9 = 00H	Fourth screen block start address
	P10 = 00H	Set to 0000H
		
5	HDOT SCR	
	C = 5AH	
	P1 = 00H	Set horizontal pixel shift to zero

(continued)

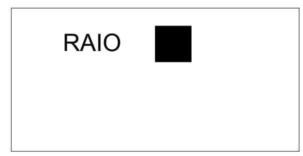
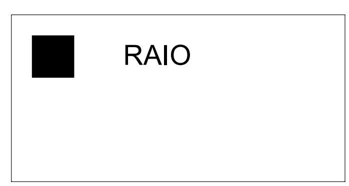
Table-25: Initialization Procedure (continued)

No.	Command	Operation
6	OVLAY C = 5BH P1 = 01H	 MX 1, MX 0: Inverse video superposition DM 1: First screen block is text mode DM 2: Third screen block is text mode
7	DISP ON/OFF C = 58H P1 = 56H	 D: Display OFF FC1, FC0: Flash cursor at 2 Hz FP1, FP0: First screen block ON FP3, FP2: Second and fourth screen blocks ON FP5, FP4: Third screen block ON
8	Clear data in first layer	Fill first screen layer memory with 20H (space character)
9	Clear data in second layer	Fill second screen layer memory with 00H (blank data) 
10	CSRW C = 46H P1 = 00H P2 = 00H	 Set cursor to start of first screen block
11	CSR FORM C = 5DH P1 = 04H P2 = 86H	 CRX: Horizontal cursor size = 5 pixels CRY: Vertical cursor size = 7 pixels CM: Block cursor
12	DISP ON/OFF C = 59H	Display ON 
13	CSR DIR	

	C = 4CH	Set cursor shift direction to right

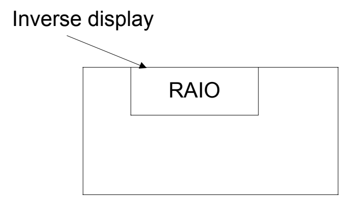
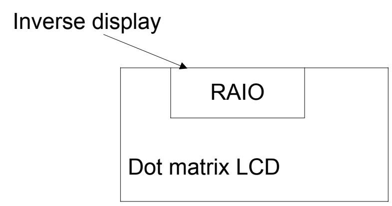
(continued)

Table-25: Initialization Procedure (continued)

No.	Command	Operation
14	MWRITE	
	C = 42H	
	P1 = 20H	' '
	P2 = 52H	'R'
	P3 = 41H	'A'
	P4 = 49H	'I'
	P5 = 4FH	'O'
		
15	CSRW	
	C = 46H	
	P1 = 00H	Set cursor to start of second screen block
	P2 = 10H	
16	CSR DIR	
	C = 4FH	Set cursor shift direction to down
17	MWRITE	
	C = 42H	
	P1 = FFH	Fill a square to the left of the 'E'
	↓	
	P9 = FFH	
		
18	CSRW	
	C = 46H	
	P1 = 01H	Set cursor address to 1001H
	P2 = 10H	
19	MWRITE	
	C = 42H	
	P1 = FFH	Fill in the second screen block in the second column of line 1
	↓	
	P9 = FFH	

(continued)

Table-25: Initialization Procedure (continued)

No.	Command	Operation
20 ↓ 29	CSRW MWRITE	Repeat operations 18 and 19 to fill in the background under 'RAIO' 
30	CSRW C = 46H P1 = 00H P2 = 01H	Set cursor to line three of the first screen block
31	CSR DIR C = 4CH	Set cursor shift direction to right
32	MWRITE C = 42H	
	P1 = 44H	'D' 
	P2 = 6FH	'o'
	P3 = 74H	't'
	P4 = 20H	' '
	P5 = 4DH	'M'
	P6 = 61H	'a'
	P7 = 74H	't'
	P8 = 72H	'r'
	P9 = 69H	'i'
	P10 = 78H	'x'
	P11 = 20H	' '
	P12 = 4CH	'L'
	P13 = 43H	'C'
	P14 = 44H	'D'

8-1-3 Display Mode Setting Example 1: combining text and graphics

◎ Conditions

- 320 x 200 pixels, single-panel drive (1/200 duty cycle)
- First layer: text display
- Second layer: graphics display
- 8 x 8-pixel character font
- CG RAM not required

◎ Display Memory Allocation

- First layer (text): 320/8 = 40 characters per line, 200/8 = 25 lines. Required memory size = 40 x 25 = 1000 bytes.
- Second layer (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 40 x 200 = 8000 bytes.

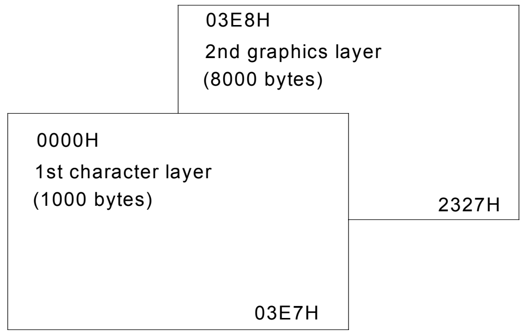


Figure 8-2: Character Over Graphics Layers

◎ Register Setup Procedure

SYSTEM SET   TC/R calculation
C = 40H
P1 = 30H f_{OSC} = 6 MHz
P2 = 87H f_{FR} = 70 Hz
P3 = 07H
P4 = 27H   (1/6) x 9 x [TC/R] x 200 = 1/70
P5 = 2FH   [TC/R] = 48, so TC/R = 2FH
P6 = C7H
P7 = 28H
P8 = 00H

SCROLL
C = 44H
P1 = 00H
P2 = 00H
P3 = C8H
P4 = E8H
P5 = 03H
P6 = C8H
P7 = XH
P8 = XH
P9 = XH
P10 = XH
CSR FORM
C = 5DH
P1 = 04H
P2 = 86H

HDOT SCR
C = 5AH
P1 = 00H

OVLAY

C = 5BH
P1 = 00H

DISP ON/OFF
C = 59H
P1 = 16H

X = Don't care

8-1-4 Display Mode Setting Example 2: combining graphics and graphics

◎ Conditions

- 320x200 pixels, single-panel drive (1/ 200 duty cycle)
- First layer: graphics display
- Second layer: graphics display

◎ Display Memory Allocation

- First layer (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 40x200 = 8000 bytes.
- Second layer (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 8000 bytes.

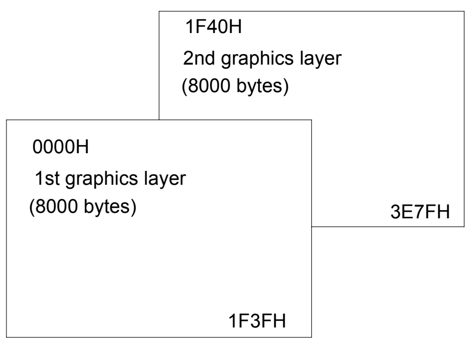


Figure 8-3: Two Layer Graphics

◎ Register Setup Procedure

SYSTEM SET TC/R calculation
C = 40H
P1 = 30H f_{OSC} = 6 MHz
P2 = 87H f_{FR} = 70 Hz
P3 = 07H
P4 = 27H (1/6) x 9 x [TC/R] x 200 = 1/70
P5 = 2FH [TC/R] = 48, so TC/R = 2FH
P6 = C7H
P7 = 28H
P8 = 00H

SCROLL
C = 44H
P1 = 00H
P2 = 00H
P3 = C8H
P4 = 40H

P5 = 1FH
P6 = C8H
P7 = XH
P8 = XH
P9 = XH
P10 = XH

CSR FORM
C = 5DH
P1 = 07H
P2 = 87H

HDOT SCR
C = 5AH
P1 = 00H

OVLAY
C = 5BH
P1 = 0CH

DISP ON/OFF
C = 59H
P1 = 16H

X = Don't care

8-1-5 Display Mode Setting Example 3: combining three graphics layers

◎ Conditions

- 320x200 pixels, single-panel drive (1/200 duty cycle)
- First layer: graphics display
- Second layer: graphics display
- Third layer: graphics display

◎ Display Memory Allocation

- All layers (graphics): 320/8 = 40 characters per line, 200/1 = 200 lines. Required memory size = 40x200 = 8000 bytes.

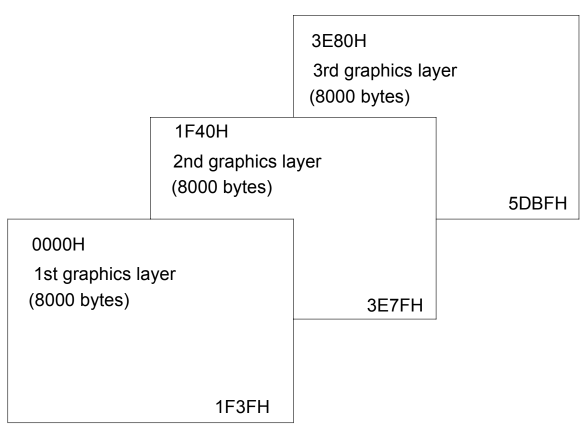


Figure 8-4: Three Layer Graphics

◎ Register Setup Procedure

SYSTEM	SET TC/R calculation
C = 40H	
P1 = 30H	f_{OSC} = 6 MHz
P2 = 87H	f_{FR} = 70 Hz
P3 = 07H	
P4 = 27H	(1/6) x 9 x [TC/R] x 200 = 1/70
P5 = 2FH	[TC/R] = 48, so TC/R = 2FH
P6 = C7H	
P7 = 28H	
P8 = 00H	

SCROLL
C = 44H
P1 = 00H
P2 = 00H
P3 = C8H
P4 = 40H
P5 = 1FH
P6 = C8H
P7 = 80H
P8 = 3EH
P9 = XH
P10 = XH
CSR FORM
C = 5DH
P1 = 07H
P2 = 87H

HDOT SCR
C = 5AH
P1 = 00H

OVLAY
C = 5BH
P1 = 1CH

DISP ON/OFF
C = 59H
P1 = 16H

X = Don't care

8-2 System Overview

Figure 8-5 shows the RA8835 series in a typical system. The microprocessor issues instructions to the RA8835 series, and the RA8835 series drives the LCD panel and may have up to 64KB of display memory. Since all of the LCD control circuits are integrated onto the RA8835 series, few external components are required to construct a complete medium- resolution liquid crystal display.

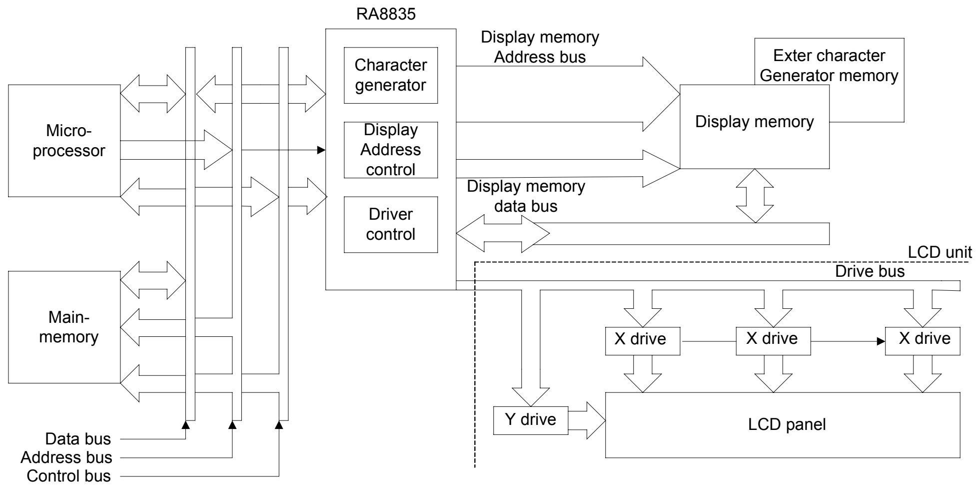


Figure 8-5: System Block Diagram

8-3 System Interconnection

8-3-1 RA8835

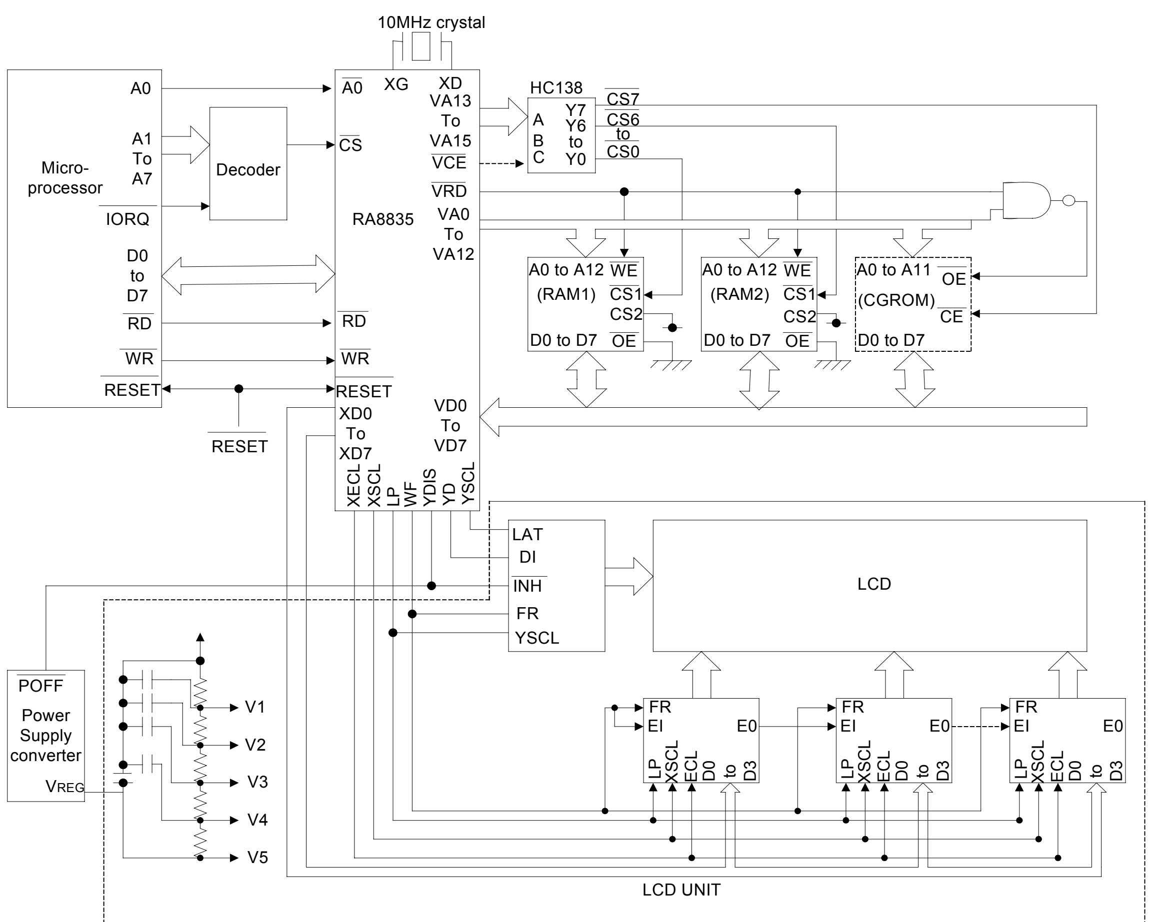


Figure 8-6: System Interconnection Diagram

The RA8835 series layered screens and flexible scrolling facilities support a range of display functions and reduces the load on the controlling microprocessor when displaying underlining, inverse display, text overlaid on graphics or simple animation.
These facilities are supported by the RA8835 series ability to divide display memory into up to four different areas.

◎ Character code table
- Contains character codes for text display
- Each character requires 8 bits
- Table mapping can be changed by using the scroll start function

◎ Graphics data table
- Contains graphics bitmaps
- Word length is 8 bits
- Table mapping can be changed

◎ CG RAM table
- Character generator memory can be modified by the external microprocessor
- Character sizes up to 8x16-pixels (16 bytes per character)
- Maximum of 64 characters
- Table mapping can be changed

◎ CG ROM table
- Used when the internal character generator is not adequate
- Can be used in conjunction with the internal character generator and external character generator RAM
- Character sizes up to 8x16-pixels (16 bytes per character)
- Maximum of 256 characters
- Fixed mapping at F000H to FFFFH

8-4 Smooth Horizontal Scrolling

Figure 8-7 illustrates smooth display scrolling to the left. When scrolling left, the screen is effectively moving to the right, over the larger virtual screen. Instead of changing the display start address SAD and shifting the display by eight pixels, smooth scrolling is achieved by repeatedly changing the pixel-shift parameter of the HDOT SCR command. When the display has been scrolled seven pixels, the HDOT SCR pixel-shift parameter is reset to zero and SAD incremented by one. Repeating this operation at a suitable rate gives the appearance of smooth scrolling.

To scroll the display to the right, the reverse procedure is followed. When the edge of the virtual screen is reached, the microprocessor must take appropriate steps so that the display is not corrupted. The scroll must be stopped or the display modified.

Note that the HDOT SCR command cannot be used to scroll individual layers.

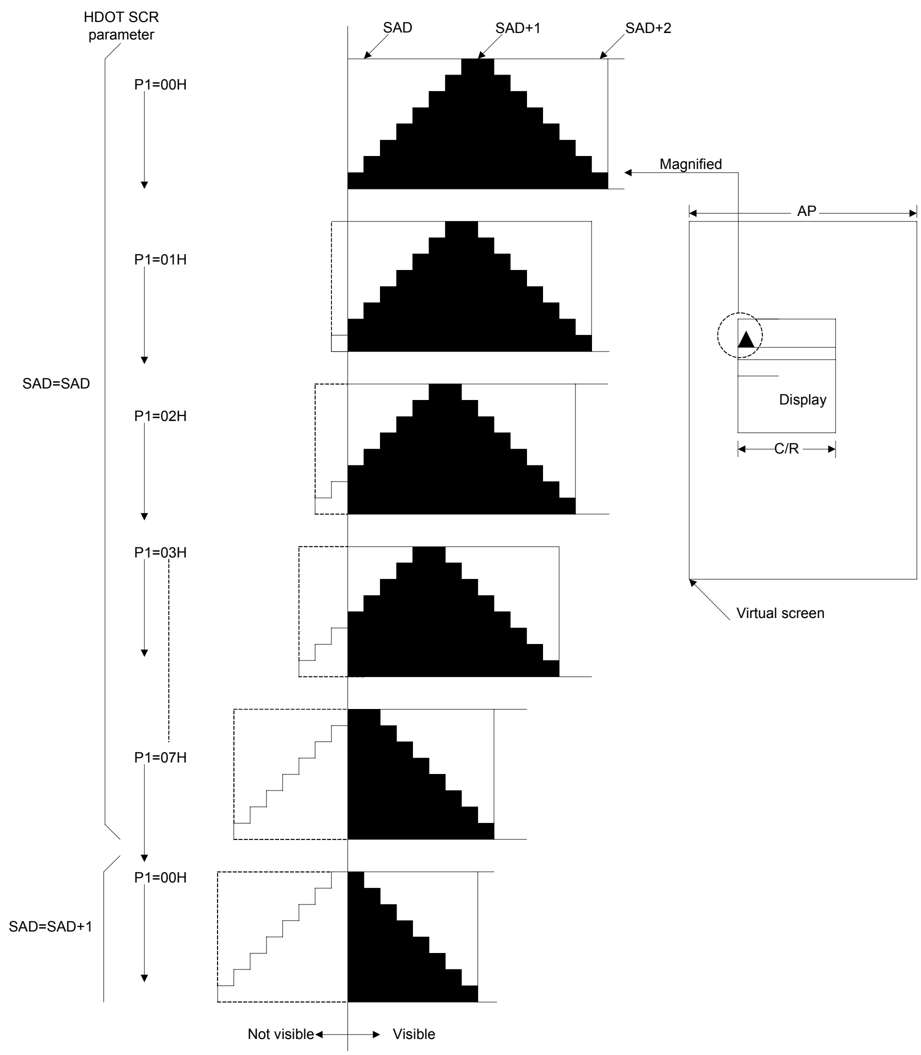


Figure: 8-7 HDOT SCR Example

Note: The response time of LCD panels changes considerably at low temperatures. Smooth scrolling under these conditions may make the display difficult to read.

8-5 Layered Display Attributes

RA8835 series incorporates a number of functions for enhanced displays using monochrome LCD panels. It allows the display of inverse characters, half-intensity menu pads and flashing of selected screen areas. These functions are controlled by the OVLAY and DISP ON/OFF commands.

A number of means can be used to achieve these effects, depending on the display configuration. These are listed below. Note, however, that not all of these can be used in the one layer at the same time.

Attribute	MX1	MX0	Combined layer display		1st layer display		2ndt layer display
Reverse	0 1	1 1	IV	RAIO	IV	RAIO	
Half-tone	0 1	0 1	ME	Yes,No	ME	Yes, No	
Local flashing	0 0	0 1	BL	Error	BL		Error
Ruled line	0 0 1	0 1 1	RL	LINE LINE	RL	LINE LINE	

Figure 8-8: Layer Synthesis

8-5-1 Inverse Display

The first layer is text, the second layer is graphics.

1. CSRW, CSDIR, MWRITE
   Write is into the graphics screen at the area to be inverted.
2. OVLAY: MX0 = 1, MX1 = 0
   Set the combination of the two layers to Exclusive-OR.
3. DISP ON/OFF: FP0 = FP1 = 1, FP1 = FP3 = 0.
   Turn on layers 1 and 2.

8-5-2 Half-tone Display

The FP parameter can be used to generate half-intensity display by flashing the display at 17 Hz. Note that this mode of operation may cause flicker problems with certain LCD panels.

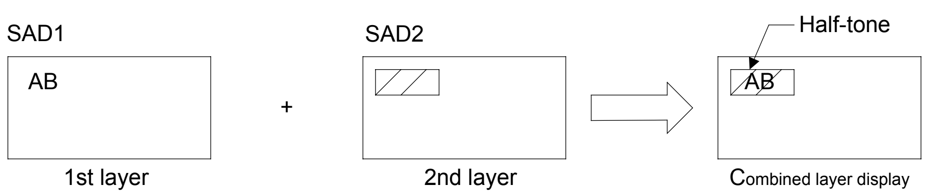


Figure 8-9: Half-tone Character and Graphics

8-5-2-1 Menu pad display

1. OVLAY: P1 = 00H
2. DISP ON/OFF: P1 = 34H

8-5-2-2 Graph display

To present two overlaid graphs on the screen, configure the display as for the menu bar display

and put one graph on each screen layer. The difference in contrast between the half- and full-intensity displays will make it easy to distinguish between the two graphs and help create an attractive display.

1. OVLAY: P1 = 00H
2. DISP ON/OFF: P1 = 34H

8-5-3 Flashing Area

8-5-3-1 Small area

To flash selected characters, the MPU can alternately write the characters as character codes and blank characters at intervals of 0.5 to 1.0 seconds.

8-5-3-1 Large area

Divide layer 1 and layer 2 into two screen blocks each, layer 2 being divided into the area to be flashed and the remainder of the screen. Flash the layer 2 screen block at 2 Hz for the area to be flashed and combine the layers using the OR function.

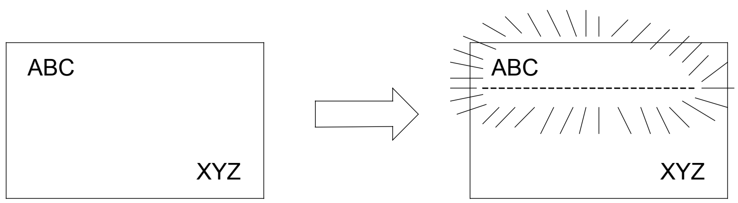


Figure 8-10: Localized Flashing

8-6 16 x 16-dot Graphic Display

8-6-1 Command Usage

This example shows how to display 16 x 16-pixel characters. The command sequence is as follows:

CSRW	Set the cursor address.
CSRDIR	Set the cursor auto-increment direction.
MWRITE	Write to the display memory.

8-6-2 Kanji Character Display

The program for writing large characters operates as follows:

1. The microprocessor reads the character data from its ROM.
2. The microprocessor sets the display address and writes to the VRAM. The flowchart is shown in Figure 8-13.

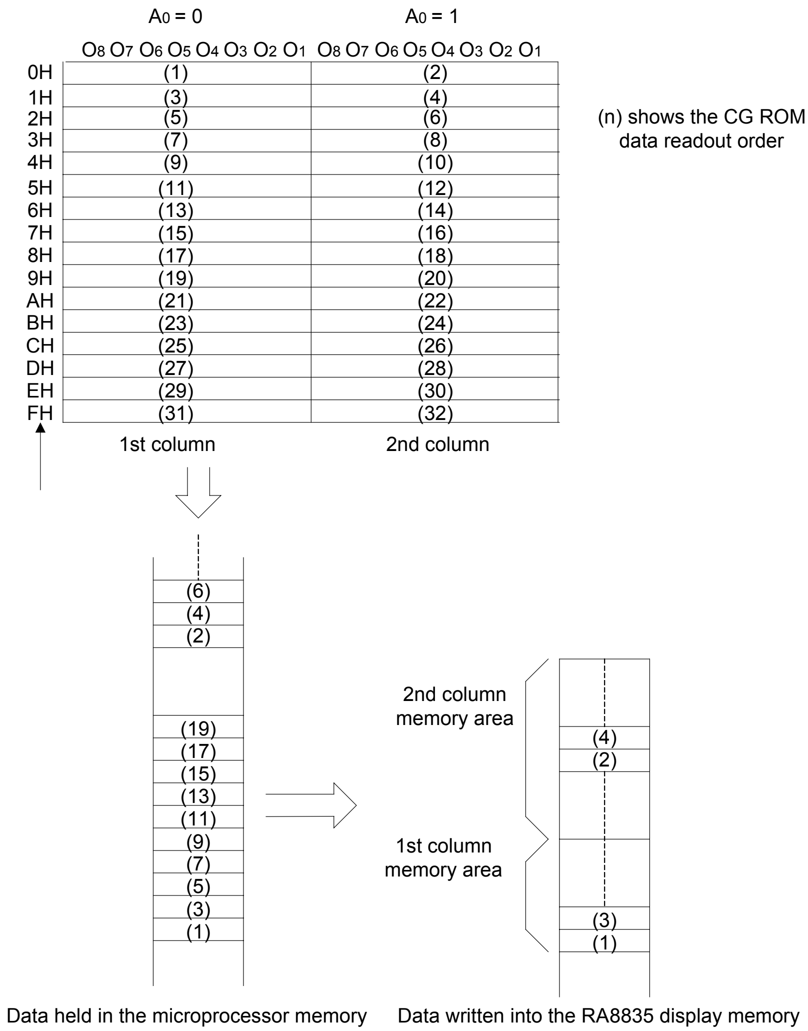


Figure 8-11: Graphics Address Indexing

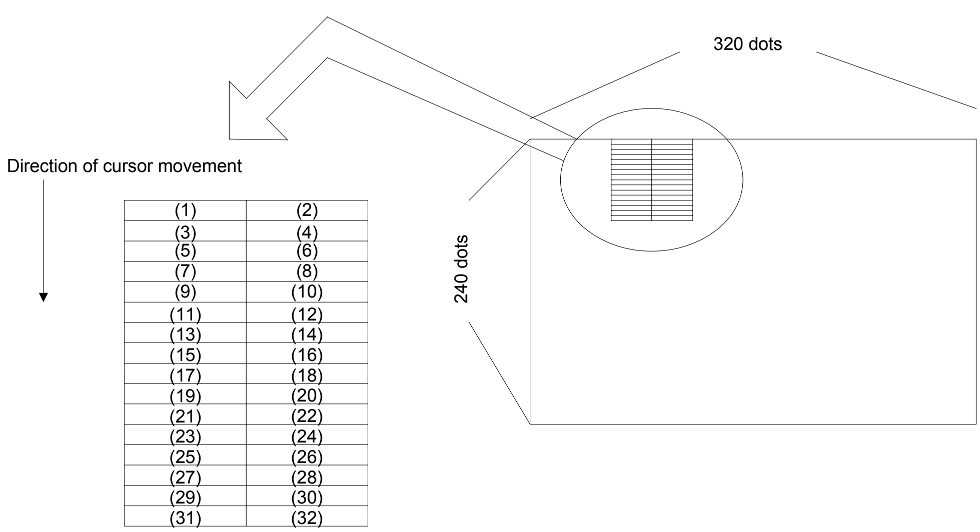


Figure 8-12: Graphics Bit Map

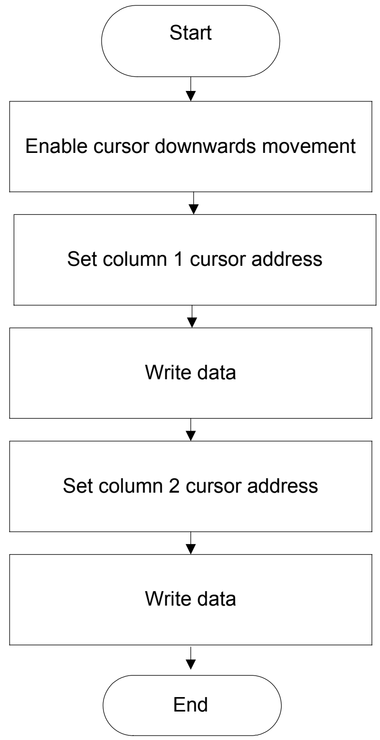


Figure 8-13: 16 x16-dot Display Flowchart

Using an external character generator ROM, and 8 x 16 pixel font can be used, allowing a 16 x 16-pixel character to be displayed in two segments. The external CG ROM EPROM data format is described in Section 10-1. This will allow the display of up to 128, 16 x 16-pixel characters. If CG RAM is also used, 96 fixed characters and 32 bank-switchable characters can also be supported.

8-7 Internal Character Generator Font

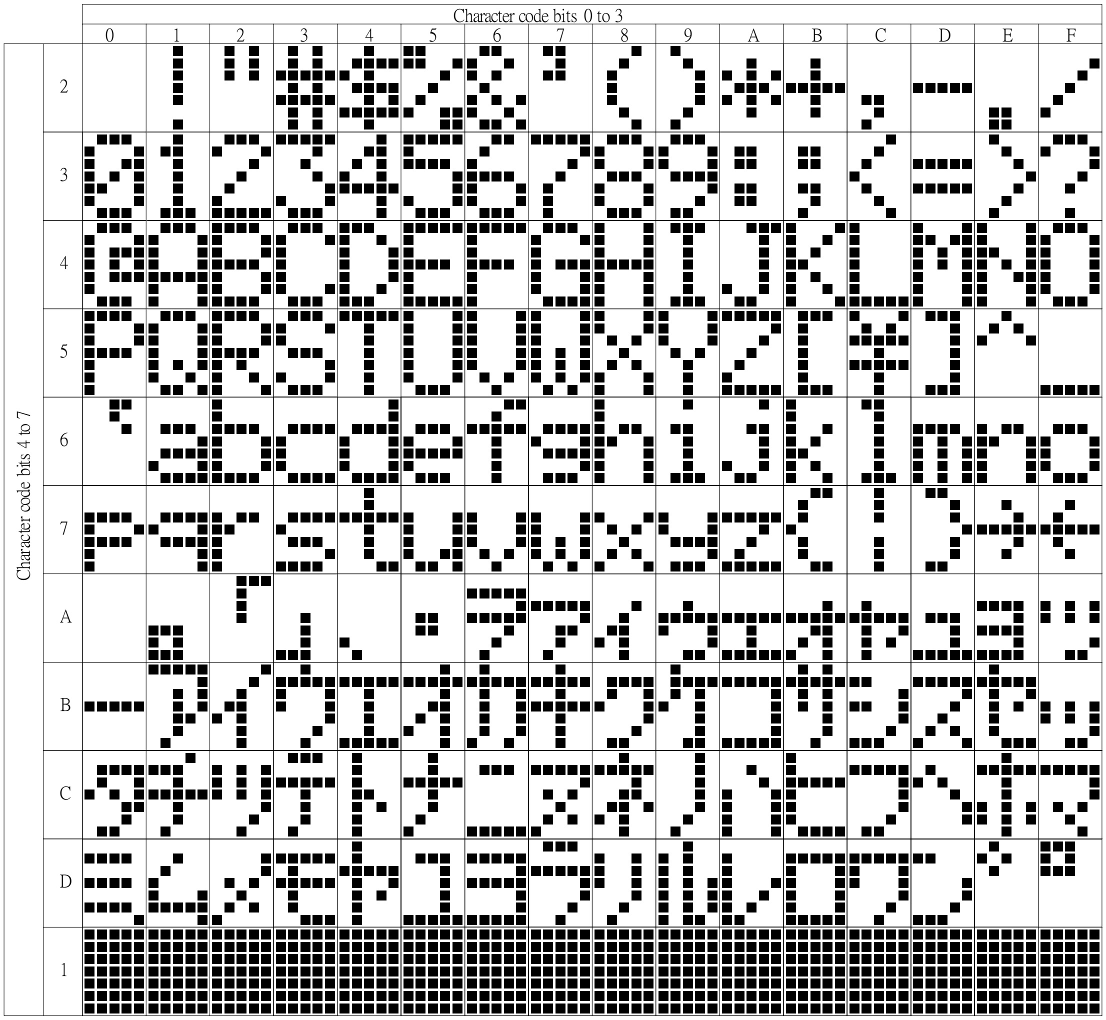
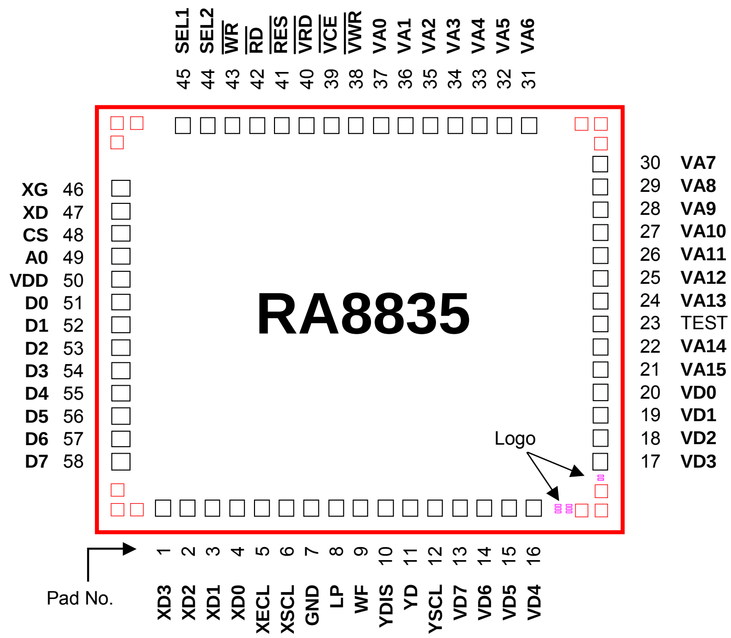


Figure 8-14: On-chip Character Set

Note: The shaded positions indicate characters that have the whole 6 x 8 bitmap blackened.

9. Package Dimensions

9-1 Die Form

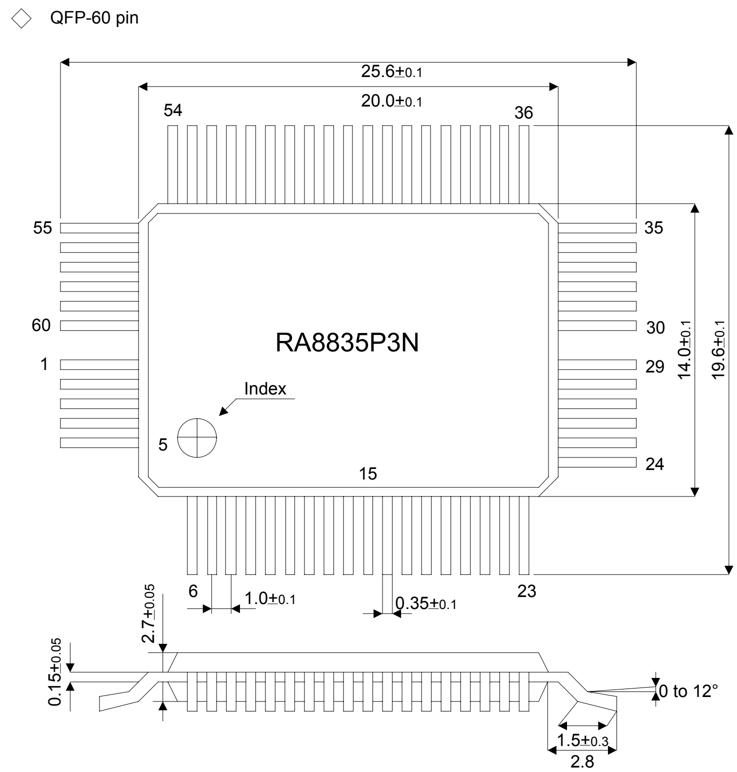


9-2 XY Coordinate

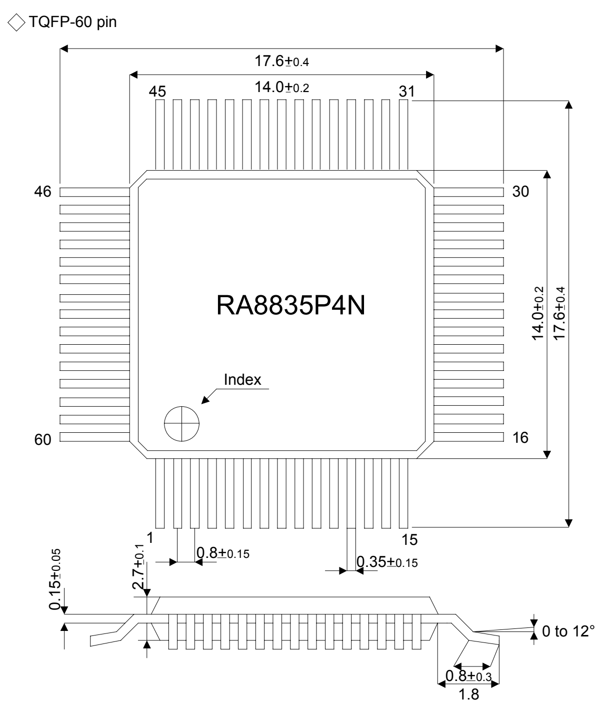
Pad No.	Pad 名稱	X 座標	Y 座標
1	XD3	-783.5	-921.4
2	XD2	-682.5	-921.4
3	XD1	-581.5	-921.4
4	XD0	-480.5	-921.4
5	XECL	-379.5	-921.4
6	XSCL	-278.5	-921.4
7	GND	-169.5	-921.4
8	LP	-64.5	-921.4
9	WF	36.5	-921.4
10	YDIS	137.5	-921.4
11	YD	238.5	-921.4
12	YSCL	339.5	-921.4
13	VD7	440.5	-921.4
14	VD6	541.5	-921.4
15	VD5	642.5	-921.4
16	VD4	743.5	-921.4
17	VD3	1043.4	-661.5
18	VD2	1043.4	-560.5
19	VD1	1043.4	-459.5
20	VD0	1043.4	-358.5
21	VA15	1043.4	-257.5
22	VA14	1043.4	-156.5
23	TEST	1043.4	-55.5
24	VA13	1043.4	45.5
25	VA12	1043.4	146.5
26	VA11	1043.4	247.5
27	VA10	1043.4	348.5
28	VA9	1043.4	449.5
29	VA8	1043.4	550.5
30	VA7	1043.4	651.5

Pad No.	Pad 名稱	X 座標	Y 座標
31	VA6	743.5	921.4
32	VA5	634.5	921.4
33	VA4	525.5	921.4
34	VA3	416.5	921.4
35	VA2	306.5	921.4
36	VA1	197.5	921.4
37	VA0	88.5	921.4
38	$\overline{VWR}$	-20.5	921.4
39	$\overline{VCE}$	-129.5	921.4
40	$\overline{VRD}$	-238.5	921.4
41	$\overline{RES}$	-347.5	921.4
42	$\overline{RD}$	-456.5	921.4
43	$\overline{WR}$	-565.5	921.4
44	SEL2	-674.5	921.4
45	SEL1	-783.5	921.4
46	XG	-1043.4	597.45
47	XD	-1043.4	461.45
48	$\overline{CS}$	-1043.4	348.5
49	A0	-1043.4	247.5
50	VDD	-1043.4	146.5
51	D0	-1043.4	45.5
52	D1	-1043.4	-55.5
53	D2	-1043.4	-156.5
54	D3	-1043.4	-257.5
55	D4	-1043.4	-358.5
56	D5	-1043.4	-459.5
57	D6	-1043.4	-560.5
58	D7	-1043.4	-661.5

9-3 RA8835P3N (Unit: mm)



9-4 RA8835P4N (Unit: mm)



Note: Both of the RA8835P3N and RA8835P4N are use “lead free” process and package.

10. Specifications

10-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to VDD+ 0.3	V
Power dissipation	P_D	300	mW
Operating temperature range	Topg	–20 to 75	°C
Storage temperature range	Tstg	–65 to 150	°C
Soldering temperature (10 seconds). See note 1.	Tsolder	260	°C

Notes:

1. The humidity resistance of the flat package may be reduced if the package is immersed in solder. Use a soldering technique that does not heatstress the package.
2. If the power supply has a high impedance, a large voltage differential can occur between the input and supply voltages. Take appropriate care with the power supply and the layout of the supply lines. (See section 7-2)
3. All supply voltages are referenced to V_{SS} = 0V.

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V_{DD} = 2.7 to 5.5V, V_{SS} = 0V, Ta = –20 to 75℃

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	V
Supply voltage	V_{DD}		2.7	3.3/5.0	5.5	V
Register data retention voltage	V_{OH}		2.0	—	6.0	V
Input leakage current	I_{LI}	VI= VDD. See note 5.	—	0.05	2.0	mA
Output leakage current	I_{LO}	VI= VSS. See note 5.	—	0.10	5.0	mA
Operating supply current	Iopr	See note 4.	—	11	15	mA
Quiescent supply current	I_Q	Sleep mode, VOSC1= V($\overline{CS}$)= V($\overline{RD}$)= VDD	—	0.05	20.0	mA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 6.	1.0	—	18.0	MHz
External clock frequency	f_{CL}		1.0	—	10.0	MHz
Oscillator feedback resistance	Rf		0.5	1.0	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	$0.5V_{DD}$	—	V_{DD}	V
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	$0.2\ V_{DD}$	V
HIGH-level output voltage	V_{OHT}	IOH= –5.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	IOL= 5.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						

HIGH-level input voltage	V_{IHC}	See note 2.	0.8 V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2 V_{DD}	V
HIGH-level output voltage	V_{OHC}	IOH= –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	IOH= 1.6 mA. See note 2.	—	—	VSS+ 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	IOL= 6.0 mA.	—	—	V_{SS} + 0.4V	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5 V_{DD}	0.7 V_{DD}	0.8 V_{DD}	V
Falling-edge threshold voltage	V_{T-}	See note 3.	0.2 V_{DD}	0.3 V_{DD}	0.5 V_{DD}	V

Notes:
1. D0 to D7, A0, ($\overline{CS}$), ($\overline{RD}$), ($\overline{WR}$), VD0 to VD7, VA0 to VA15, ($\overline{VRD}$), ($\overline{VWR}$) and ($\overline{VCE}$) are TTL-level inputs.
2. SEL1 is CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS are CMOS-level outputs.
3. $\overline{RES}$ is an Schmitt-trigger input. The pulse width on ($\overline{RES}$) must be at least 200us. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. f_{OSC} = 10 MHz, no load (no display memory), internal character generator, 256x200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
6. Because the oscillator circuit input bias current is in the order of uA, design the printed circuit board so as to reduce leakage currents.

V_{DD} = 2.7 to 4.5V, V_{SS} = 0V, Ta = –20 to 75℃

Parameter	Symbol	Condition	Rating			Unit
			Min.	**Typ.**	**Max.**	V
Supply voltage	V_{DD}		2.7	3.5	4.5	V
Register data retention voltage	V_{OH}		2.0	—	6.0	V
Input leakage current	I_{LI}	$V_I = V_{DD}$. See note 5.	—	0.05	2.0	mA
Output leakage current	I_{LO}	$V_I = V_{SS}$. See note 5.	—	0.10	5.0	mA
Operating supply current	Iopr	V_{DD} = 3.5 V. See note 4.	—	3.5	—	mA
		See note 4.	—	—	7.0	
Quiescent supply current	I_Q	Sleep mode, $V_{OSC1} = V_{CS} = V_{RD} = V_{DD}$	—	0.05	20.0	mA
Oscillator frequency	f_{OSC}	Measured at crystal, 47.5% duty cycle. See note 6.	1.0	—	8.0	MHz
External clock frequency	f_{CL}		1.0	—	8.0	MHz
Oscillator feedback resistance	Rf		0.7	—	3.0	MΩ
TTL						
HIGH-level input voltage	V_{IHT}	See note 1.	0.5 V_{DD}	—	V_{DD}	V

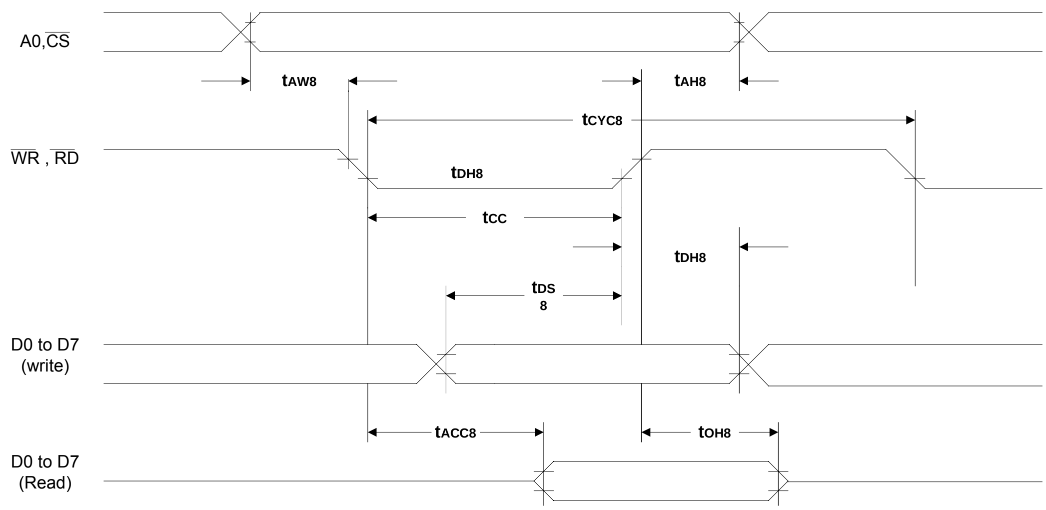
LOW-level input voltage	V_{ILT}	See note 1.	V_{SS}	—	0.2 V_{DD}	V
HIGH-level output voltage	V_{OHT}	I_{OH} = –3.0 mA. See note 1.	2.4	—	—	V
LOW-level output voltage	V_{OLT}	I_{OL} = 3.0 mA. See note 1.	—	—	V_{SS} + 0.4	V
CMOS						
HIGH-level input voltage	V_{IHC}	See note 2.	0.8 V_{DD}	—	V_{DD}	V
LOW-level input voltage	V_{ILC}	See note 2.	V_{SS}	—	0.2 V_{DD}	V
HIGH-level output voltage	V_{OHC}	I_{OH} = –2.0 mA. See note 2.	V_{DD} – 0.4	—	—	V
LOW-level output voltage	V_{OLC}	I_{OH} = 1.6 mA. See note 2.	—	—	V_{SS} + 0.4	V
Open-drain						
LOW-level output voltage	V_{OLN}	I_{OL} = 6.0 mA.	—	—	V_{SS} + 0.4	V
Schmitt-trigger						
Rising-edge threshold voltage	V_{T+}	See note 3.	0.5 V_{DD}	0.7 V_{DD}	0.8 V_{DD}	V
Falling-edge threshold voltage	V_{T-}	See note 3.	0.2 V_{DD}	0.3 V_{DD}	0.5 V_{DD}	V

Notes

1. D0 to D7, A0, ($\overline{CS}$), ($\overline{RD}$), ($\overline{WR}$), VD0 to VD7, VA0 to VA15, ($\overline{VRD}$), ($\overline{VWR}$) and ($\overline{VCE}$) are TTL-level inputs.
2. SEL1 is CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, $\overline{WF}$, YDIS are CMOS-level outputs.
3. $\overline{RES}$ is an Schmitt-trigger input. The pulse width on ($\overline{RES}$) must be at least 200 s. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
4. f_{OSC} = 10 MHz, no load (no display memory), internal character generator, 256 . 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
6. Because the oscillator circuit input bias current is in the order of A, design the printed circuit board so as to reduce leakage currents.

10-3 RA8835 Timing Diagrams

10-3-1 8080 Family Interface Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
A0, $\overline{CS}$	t_{AH8}	Address hold time	10	—	10	—	ns	CL = 100pF
	t_{AW8}	Address setup time	0	—	0	—	ns	
$\overline{WR}$, $\overline{RD}$	t_{CYC8}	System cycle time	note.	—	note.	—	ns	
	t_{CC}	Strobe pulse width	120	—	150	—	ns	
D0 to D7	t_{DS8}	Data setup time	120	—	120	—	ns	
	t_{DH8}	Data hold time	5	—	5	—	ns	
	t_{ACC8}	$\overline{RD}$ access time	—	50	—	80	ns	
	t_{OH8}	Output disable time	10	50	10	55	ns	

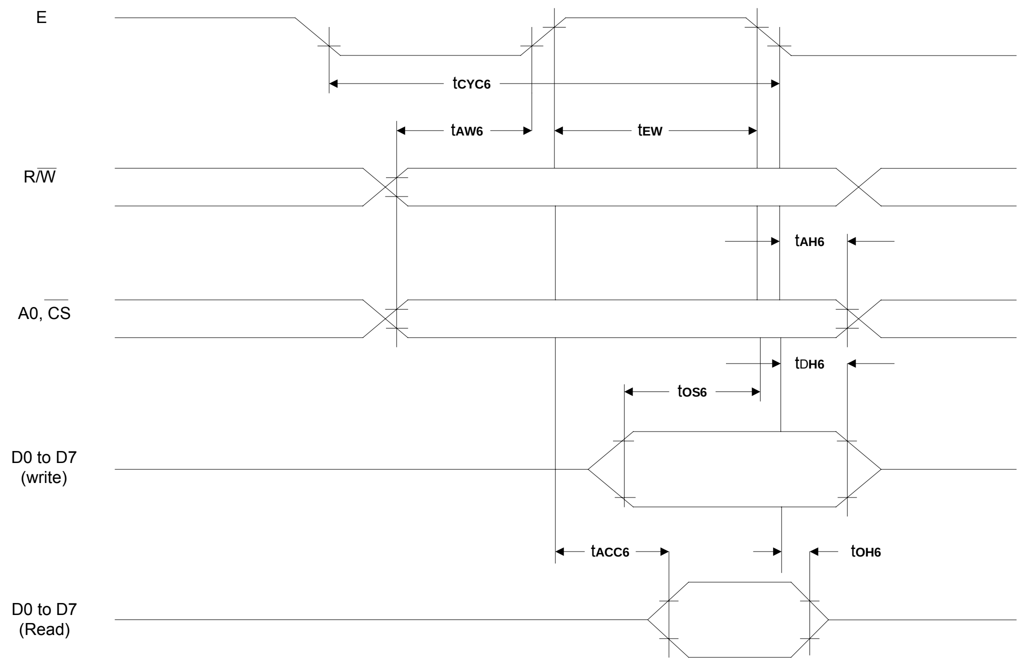
Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

10-3-2 6800 Family Interface Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
A0, $\overline{CS}$, R/(/W)	t_{CYC6}	System cycle time	note.	—	note.	—	ns	CL = 100 pF
	t_{AW6}	Address setup time	0	—	10	—	ns	
	t_{AH6}	Address hold time	0	—	0	—	ns	
D0 to D7	t_{DS6}	Data setup time	100	—	120	—	ns	
	t_{DH6}	Data hold time	0	—	0	—	ns	
	t_{OH6}	Output disable time	10	50	10	75	ns	
	t_{ACC6}	Access time	—	85	—	130	ns	
E	t_{EW}	Enable pulse width	120	—	150	—	ns	

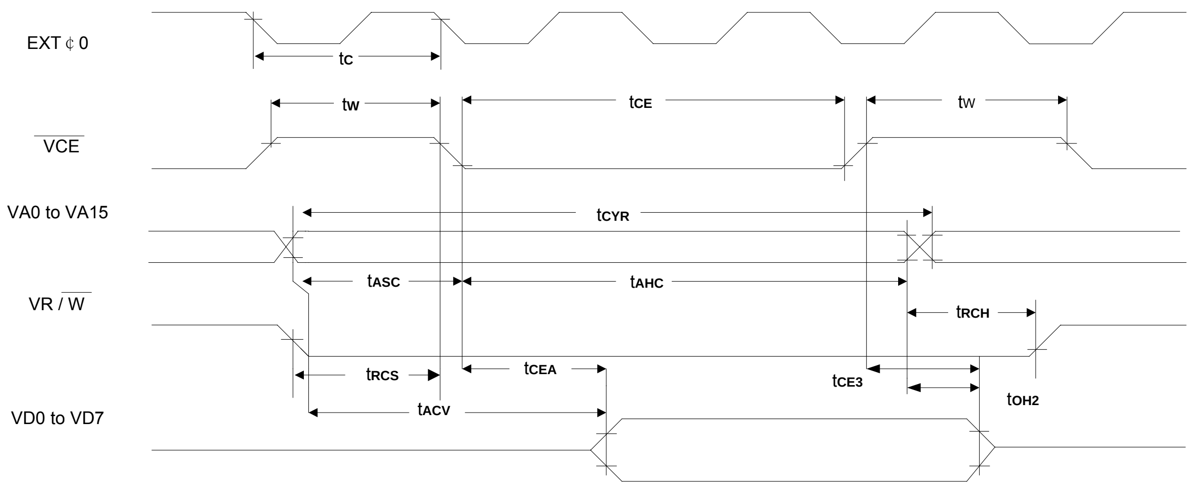
Note: For memory control and system control commands:

$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

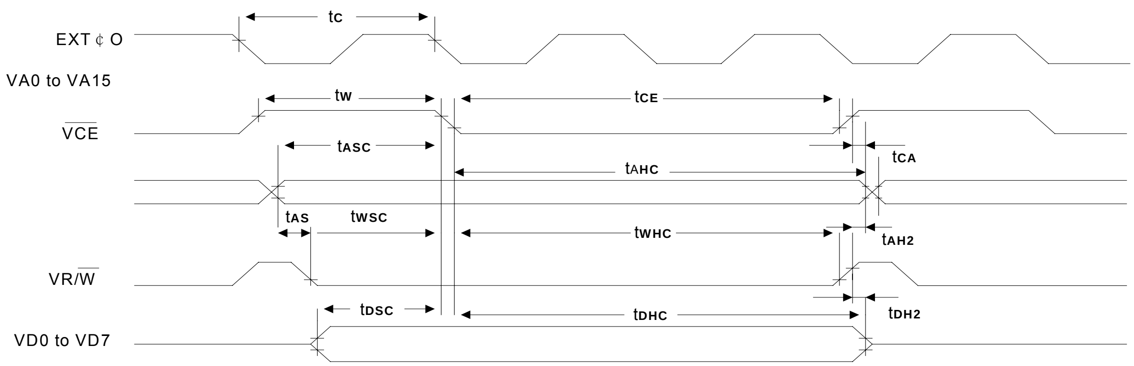
10-3-3 Display Memory Read Timing



Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse width	$2t_C$ – 30	—	2 t_C – 30	—	ns	
VA0 to VA15	t_{CYR}	Read cycle time	$3t_C$	—	$3t_C$	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 100	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	2 t_C – 30	—	$2t_C$ – 40	—	ns	
$\overline{VRD}$	t_{RCS}	Read cycle setup time to falling edge of $\overline{VCE}$	t_C – 45	—	t_C – 60	—	ns	
	t_{RCH}	Read cycle hold time from rising edge of $\overline{VCE}$	$0.5t_C$	—	$0.5t_C$	—	ns	
VD0 to VD7	t_{ACV}	Address access time	—	$3t_C$ – 100	—	$3t_C$ – 115	Ns	
	t_{CEA}	$\overline{VCE}$ access time	—	$2t_C$ – 80	—	$2t_C$ – 90	Ns	
	t_{OH2}	Output data hold time	0	—	0	—	ns	
	t_{CE3}	$\overline{VCE}$ to data off time	0	—	0	—	ns	

10.3-4 Display Memory Write Timing



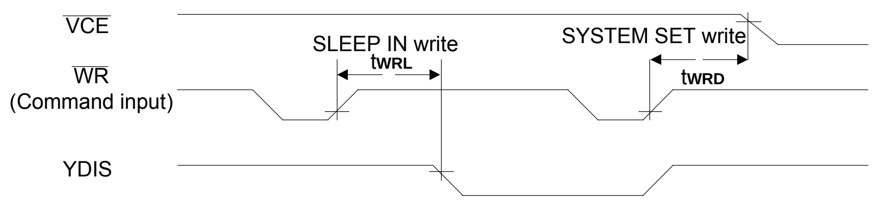
Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t_C	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	t_W	$\overline{VCE}$ HIGH-level pulse width	t_C – 50	—	t_C – 50	—	ns	
	t_{CE}	$\overline{VCE}$ LOW-level pulse width	2t_C – 30	—	2t_C – 30	—	ns	
VA0 to VA15	t_{CYW}	Write cycle time	3tC	—	3t_C	—	ns	
	t_{AHC}	Address hold time from falling edge of $\overline{VCE}$	2t_C – 30	—	2t_C – 40	—	ns	
	t_{ASC}	Address setup time to falling edge of $\overline{VCE}$	t_C – 70	—	t_C – 110	—	ns	
	t_{CA}	Address hold time from rising edge of $\overline{VCE}$	0	—	0	—	ns	
	t_{AS}	Address setup time to falling edge of $\overline{VWR}$	0	—	0	—	ns	
	t_{AH2}	Address hold time from rising edge of $\overline{VWR}$	10	—	10	—	ns	
$\overline{VWR}$	t_{WSC}	Write setup time to falling edge of $\overline{VCE}$	t_C – 80	—	t_C – 115	—	ns	
	t_{WHC}	Write hold time from falling edge of $\overline{VCE}$	2t_C – 20	—	2t_C – 20	—	ns	
VD0 to VD7	t_{DSC}	Data input setup time to falling edge of $\overline{VCE}$	t_C – 85	—	t_C – 125	—	ns	
	t_{DHC}	Data input hold time from falling edge of $\overline{VCE}$	2t_C – 30	—	2t_C – 30	—	ns	

	t_{DH2}	Data hold time from rising edge of $\overline{VWR}$	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

10-3-5 SLEEP IN Command Timing



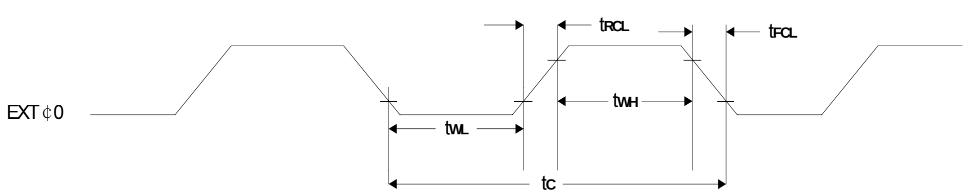
Ta = –20 to 75°C

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
$\overline{WR}$	t_{WRD}	$\overline{VCE}$ falling-edge delay time	note 1.	—	note 1.	—	ns	CL = 100 pF
	t_{WRL}	YDIS falling-edge delay time	—	note 2.	—	note 2.	ns	

Notes:

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C \cdot [TC/R] \cdot [L/F] + 70$

10-3-6 External Oscillator Signal Timing



Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V		V_{DD} = 2.7 to 4.5V		Unit	Condition
			Min.	Max.	Min.	Max.		
EXT Φ0	t_{RCL}	External clock rise time	—	15	—	15	ns	
	t_{FCL}	External clock fall time	—	15	—	15	ns	
	t_{WH}	External clock HIGH-level pulse width	note 1.	note 2.	note 1.	note 2.	ns	

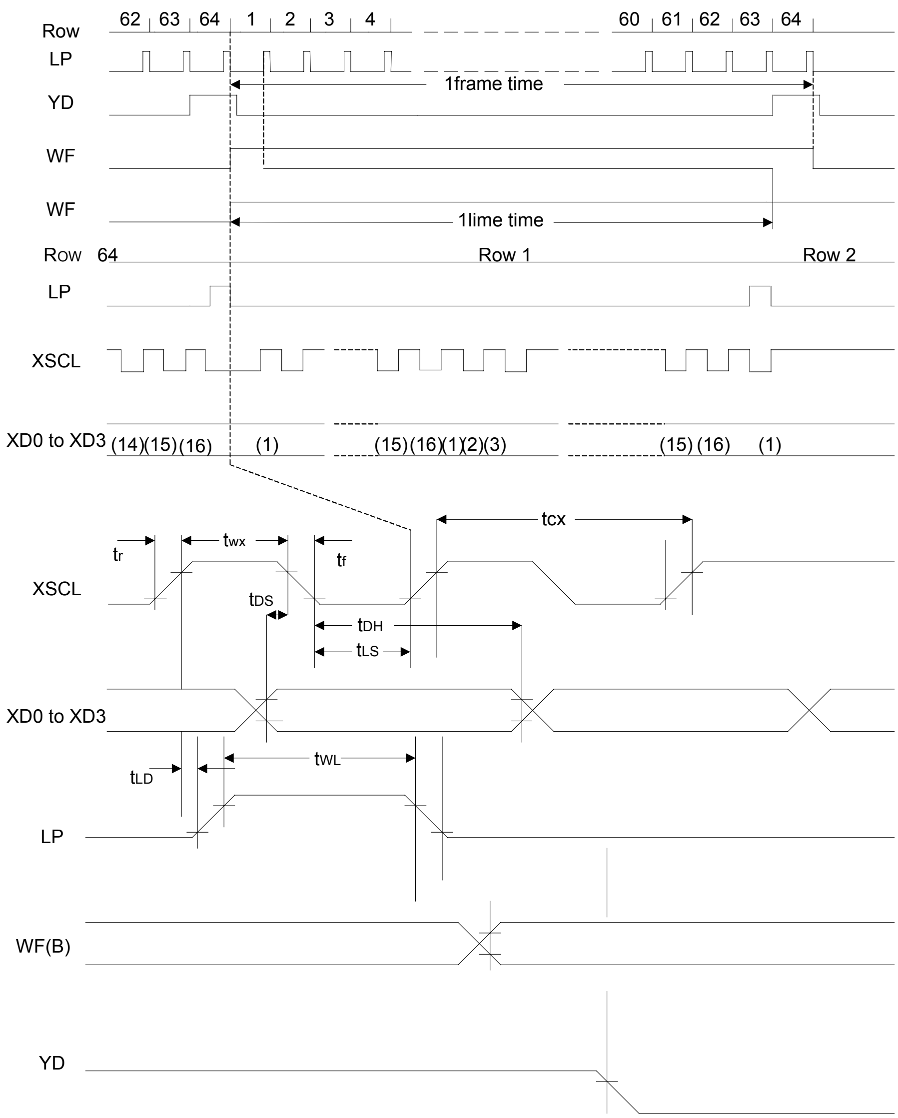
	t_{WL}	External clock LOW-level pulse width	note 1.	note 2.	note 1.	note 2.	ns	
	t_C	External clock period	100	—	125	—	ns	

Notes:

1. $(t_C - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$
2. $(t_C - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

10-3-7 LCD Output Timing

The following characteristics are for a 1/64 duty cycle.



Ta = –20 to 75℃

Signal	Symbol	Parameter	V_{DD} = 4.5 to 5.5V	V_{DD} = 2.7 to 4.5V	Unit	Condition

			Min.	Max.	Min.	Max.		
	t_r	Rise time	—	30	—	40	ns	CL = 100 pF
	t_f	Fall time	—	30	—	40	ns	
XSCL	t_{CX}	Shift clock cycle time	$4t_C$	—	$4t_C$	—	ns	
	t_{WX}	XSCL clock pulse width	$2t_C – 60$	—	$2t_C – 60$	—	ns	
XD0 to XD3	t_{DH}	X data hold time	$2t_C – 50$	—	$2t_C – 50$	—	ns	
	t_{DS}	X data setup time	$2t_C – 100$	—	$2t_C – 105$	—	ns	
LP	t_{LS}	Latch data setup time	$2t_C – 50$	—	$2t_C – 50$	—	ns	
	t_{WL}	LP pulse width	$4t_C – 80$	—	$4t_C – 120$	—	ns	
	t_{LD}	LP delay time from XSCL	0	—	0	—	ns	
WF	t_{DF}	Permitted WF delay	—	50	—	50	ns	
YD	t_{DHY}	Y data hold time	$2t_C – 20$	—	$2t_C – 20$	—	ns	